Precision Dual Output, High Current, Low Noise, Voltage Reference

FEATURES

- **Dual Output Tracking Reference**
  - Each Output Configurable: 2.5V to 6V
  - Output 1: 150mA Source/20mA Sink
  - Output 2: 50mA Source/20mA Sink
- **Low Drift:**
  - **A-Grade: 10ppm/°C Max**
  - **B-Grade: 20ppm/°C Max**
- **High Accuracy:**
  - **A-Grade: ±0.05% Max**
  - **B-Grade: ±0.1% Max**
- **Low Noise: 1.5ppm$_{P-P}$ (0.1Hz to 10Hz)**
- **Wide Operating Voltage Range to 36V**
- **Load Regulation: 0.1ppm/mA**
- AC PSRR: 96dB at 10kHz
- Kelvin Sense Connection on Outputs
- Thermal Shutdown
- Separate Supply Pins for Each Output
- Available in Exposed Pad Package MSE16

APPLICATIONS

- Microcontroller with ADC/DAC Applications
- Data Acquisition Systems
- Automotive Control and Monitoring
- Precision Low Noise Regulators
- Instrumentation and Process Control

DESCRIPTION

The LT®6658 precision 2.5V dual output reference combines the performance of a low drift low noise reference and a linear regulator. Both outputs are ideal for driving the precision reference inputs of high resolution ADCs and DACs, even with heavy loading while simultaneously acting as output supplies powering microcontrollers and other supporting devices. Both outputs have the same precision specifications and track each other over temperature and load. Both outputs are nominally 2.5V, however each can be configured with external resistors to give an output voltage up to 6V.

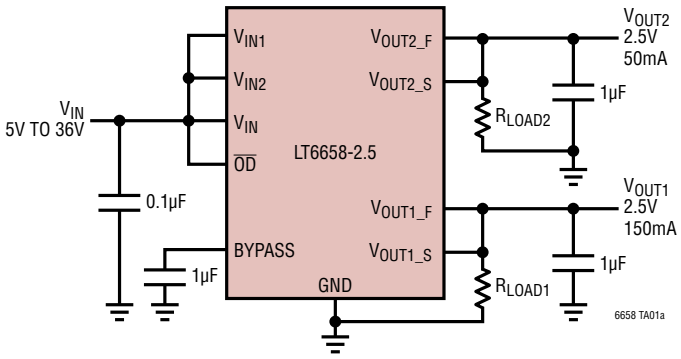
Using Kelvin connections, the LT6658 typically has 0.1ppm/mA load regulation with up to 150mA load current. A noise reduction pin is available to band-limit and lower the total integrated noise.

Dual outputs provide flexibility for powering reference and regulator applications and localizing PCB routing. The outputs have excellent supply rejection and are stable with 1µF to 50µF capacitors.

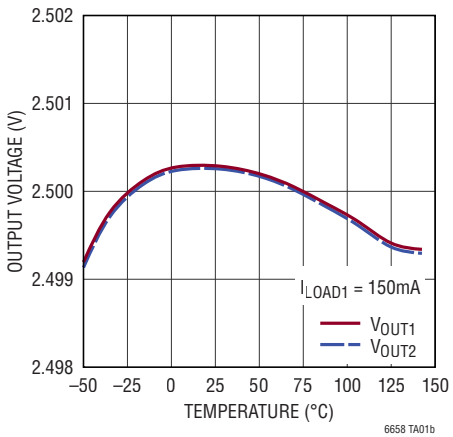
Short circuit and thermal protection help maintain stability and prevent thermal overstress. The LT6658 is offered in the MSE16 exposed pad package.

TYPICAL APPLICATION

Precision Dual Output 2.5V Reference and Supply



Output Voltage Temperature Drift Both Outputs



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- V_{IN}, V_{IN1}, V_{IN2} to GND ..... –0.3V to 38V

Input Voltages
- $\overline{OD}$ to GND ..... –0.3V to 38V
- V_{OUT1_S}, V_{OUT2_S}, NR, BYPASS to GND .. –0.3V to 6V

Output Voltages
- V_{OUT1_F}, V_{OUT2_F} to GND ..... –0.3V to 6V

Input Current
- BYPASS ..... ±10mA

Output Short-Circuit Duration ..... Indefinite

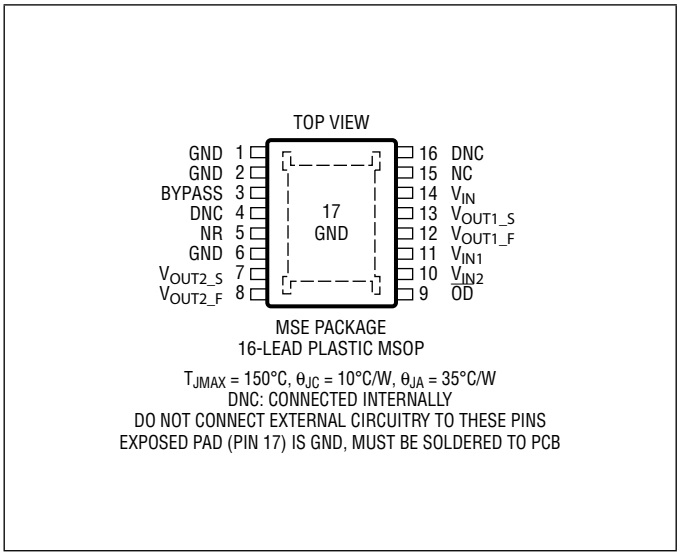
Specified Temperature Range
- I-Grade ..... –40°C to 85°C
- H-Grade ..... –40°C to 125°C

Operating Junction Temperature Range . –55°C to 150°C

Storage Temperature Range (Note 2) ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- (Note 3) ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JC} = 10°C/W, θ_{JA} = 35°C/W
DNC: CONNECTED INTERNALLY
DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT6658#orderinfo

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED JUNCTION TEMPERATURE RANGE
LT6658AIMSE-2.5#PBF	LT6658AIMSE-2.5#TRPBF	665825	16-Lead Plastic MSOP	–40°C to 85°C
LT6658BIMSE-2.5#PBF	LT6658BIMSE-2.5#TRPBF	665825	16-Lead Plastic MSOP	–40°C to 85°C
LT6658AHMSE-2.5#PBF	LT6658AHMSE-2.5#TRPBF	665825	16-Lead Plastic MSOP	–40°C to 125°C
LT6658BHMSE-2.5#PBF	LT6658BHMSE-2.5#TRPBF	665825	16-Lead Plastic MSOP	–40°C to 125°C

*The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges. Parts ending with PBF are RoHS and WEEE compliant.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AVAILABLE OPTIONS

OUTPUT VOLTAGE	INITIAL ACCURACY	TEMPERATURE COEFFICIENT	SPECIFIED JUNCTION TEMPERATURE RANGE
2.500V	0.05%	10ppm/°C	–40°C to 85°C
	0.1%	20ppm/°C	–40°C to 85°C
	0.05%	10ppm/°C	–40°C to 125°C
	0.1%	20ppm/°C	–40°C to 125°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. $V_{IN} = V_{IN1} = V_{IN2} = V_{OUT1,2\_F} + 2.5V$, $C_{OUT1,2}$ = 1µF, I_{LOAD} = 0, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Accuracy	LT6658A		–0.05		0.05	%
	LT6658B		–0.1		0.1	%
	LT6658AI	●	–0.175		0.175	%
	LT6658BI	●	–0.35		0.35	%
	LT6658AH	●	–0.215		0.215	%
	LT6658BH	●	–0.43		0.43	%
Output Voltage Temperature Coefficient (Note 4)	LT6658A	●		3	10	ppm/°C
	LT6658B	●		10	20	ppm/°C
Line Regulation (Note 5)	$V_{OUT} + 2.5V \le V_{IN} \le 36V$, $V_{IN} = V_{IN1} = V_{IN2}$			1.4	4.5	ppm/V
		●			5	ppm/V
Load Regulation (Note 5)	Output 1 Sourcing, ΔI_{LOAD} = 0mA to 150mA			0.1	0.5	ppm/mA
		●			0.8	ppm/mA
	Output 2 Sourcing, ΔI_{LOAD} = 0mA to 50mA (Note 6)			0.1	1.3	ppm/mA
		●			1.5	ppm/mA
	Output 1 Sinking, ΔI_{LOAD} = 0mA to 20mA			0.1	2.2	ppm/mA
		●			2.5	ppm/mA
	Output 2 Sinking, ΔI_{LOAD} = 0mA to 20mA			0.1	2.2	ppm/mA
		●			2.5	ppm/mA
V_{IN} Minimum Voltage	ΔV_{OUT} = 0.1%, I_{OUT} = 0mA, $V_{IN1} = V_{IN2} = V_{OUT} + 2.5V$			3.5	3.9	V
		●			4.25	V
V_{IN1} Dropout Voltage	ΔV_{OUT} = 0.1%, I_{OUT} = 0mA, $V_{IN} = V_{IN2} = V_{OUT} + 2.5V$			2.0	2.3	V
	ΔV_{OUT} = 0.1%, I_{OUT} = 150mA, $V_{IN} = V_{IN2} = V_{OUT} + 2.5V$	●		2.2	2.5	V
V_{IN2} Dropout Voltage	ΔV_{OUT} = 0.1%, I_{OUT} = 0mA, $V_{IN} = V_{IN1} = V_{OUT} + 2.5V$			1.8	2.2	V
	ΔV_{OUT} = 0.1%, I_{OUT} = 50mA, $V_{IN} = V_{IN1} = V_{OUT} + 2.5V$	●		2	2.5	V
Supply Current	$V_{\overline{OD}}$ = 5V, No Load	●		1.9	3.0	mA
	$V_{\overline{OD}}$ = 0.8V, No Load	●		1.0	1.2	mA
Output Short-Circuit Current	Short V_{OUT1_F} to GND	●	170	270		mA
	Short V_{OUT2_F} to GND	●	65	120		mA
Output Noise Voltage (Note 7)	0.1Hz ≤ f ≤ 10Hz			1.5		ppm_{P-P}
	10Hz ≤ f ≤ 1kHz, C_{OUT} = 1µF, C_{NR} = 10µF, I_{LOAD} = Full Current (Note 9)			2		ppm_{RMS}
	Frequency = 1kHz, C_{OUT1} = 1µF, C_{NR} = 10µF, I_{LOAD} = Full Current (Note 9)			8		$nV/\sqrt{Hz}$
Output Voltage Tracking	Tracking = Output 1 – Output 2			0.9		µV/°C
V_{OUT1_S}, V_{OUT2_S} Pin Current	Unity Gain			135		nA
$\overline{OD}$ Threshold Voltage	Logic High Input Voltage	●	2			V
	Logic Low Input Voltage	●			0.8	V
$\overline{OD}$ Pin Current	$V_{\overline{OD}}$ = 0V	●		30	45	µA
	$V_{\overline{OD}}$ = 36V	●		0.3	1.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{IN1} = V_{IN2} = $V_{OUT1,2\_F}$ + 2.5V, $C_{OUT1,2}$ = 1µF, I_{LOAD} = 0, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Ripple Rejection	V_{IN1} = V_{OUT1} + 3V, V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 150mA, C_{OUT1} = 1µF, C_{NR} = 10µF V_{IN2} = V_{OUT2} + 3V, V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 50mA, C_{OUT2} = 1µF, C_{NR} = 10µF			107 107		dB dB
Turn-On Time	0.1% Settling, C_{LOAD} = 1µF			160		µs
Long Term Drift (Note 8)				120		ppm/$\sqrt{kHr}$
Thermal Hysteresis (Note 9)	ΔT = –40°C to 85°C ΔT = –40°C to 125°C			30 45		ppm ppm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Thermal hysteresis can occur during storage at extreme temperatures.

Note 3: The stated temperature is typical for soldering of the leads during manual rework. For detailed IR reflow recommendations, refer to the Applications Information section.

Note 4: Temperature coefficient is measured by dividing the maximum change in output voltage by the specified temperature range.

Note 5: Line and load regulation are measured on a pulse basis for specified input voltage or load current ranges. Output changes due to die temperature change must be taken into account separately.

Note 6: V_{OUT2} load regulation specification is limited by practical automated test resolution. Please refer to the Typical Performance Characteristics section for more information regarding actual typical performance.

Note 7: Peak-to-peak noise is measured with a 1-pole highpass filter at 0.1Hz and 2-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. The test time is 10 seconds. RMS noise is measured on a spectrum analyzer in a shielded environment where the intrinsic noise of the instrument is removed to determine the actual noise of the device.

Note 8: Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours with a continuing trend toward reduced drift with time. Long-term stability will also be affected by differential stresses between the IC and the board material created during board assembly.

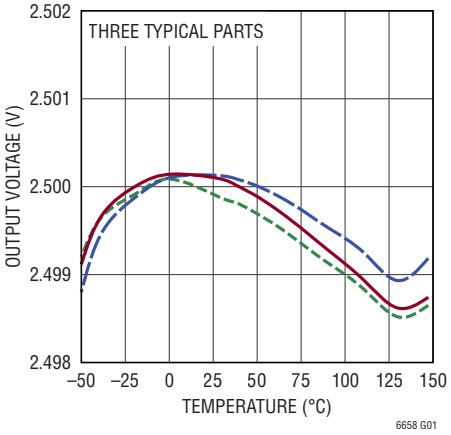
Note 9: Hysteresis in output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis measures the maximum output change for the averages of three hot or cold temperature cycles. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature), it's usually not a dominant error source. Typical hysteresis is the worst-case of 25°C to cold to 25°C or 25°C to hot to 25°C, preconditioned by one thermal cycle.

Note 10: The full current for I_{LOAD} is 150mA and 50mA for Output 1 and Output 2, respectively.

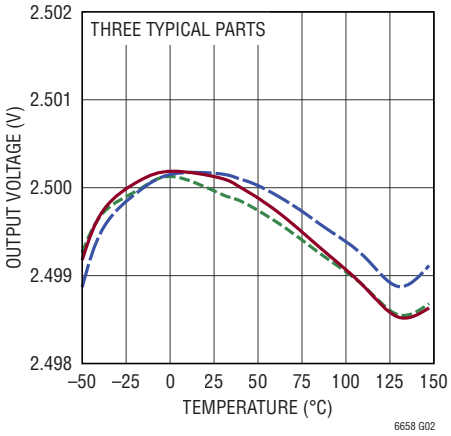
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{IN1} = V_{IN2} = V_{OUT1_F} + 2.5V = V_{OUT2_F} + 2.5V, C_{OUT1} = C_{OUT2} = 1µF, I_{LOAD} = 0mA, unless otherwise noted.

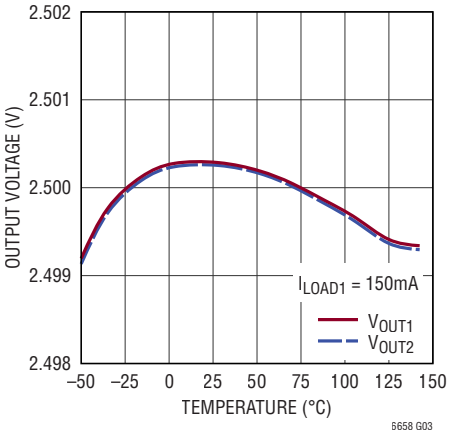
2.5V V_{OUT1} Output Voltage Temperature Drift



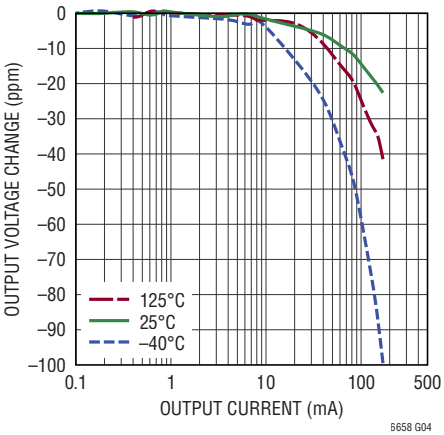
2.5V V_{OUT2} Output Voltage Temperature Drift



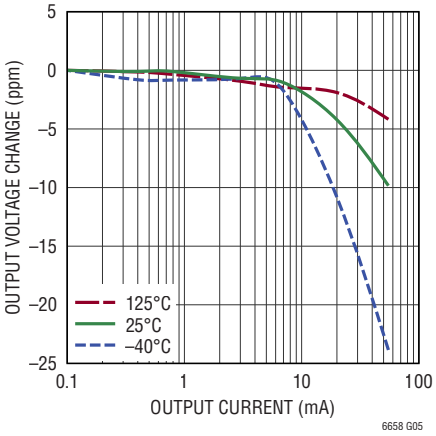
2.5V V_{OUT1} and V_{OUT2} Output Voltage vs Temperature with 150mA Load on V_{OUT1}



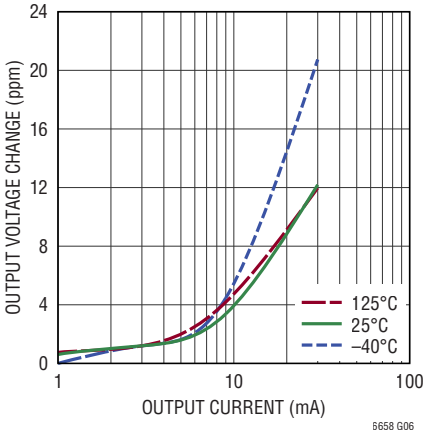
2.5V V_{OUT1} Load Regulation, Sourcing



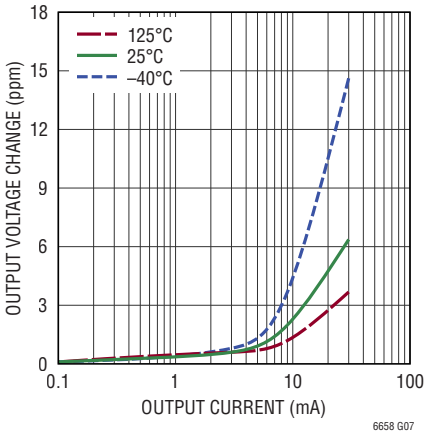
2.5V V_{OUT2} Load Regulation, Sourcing



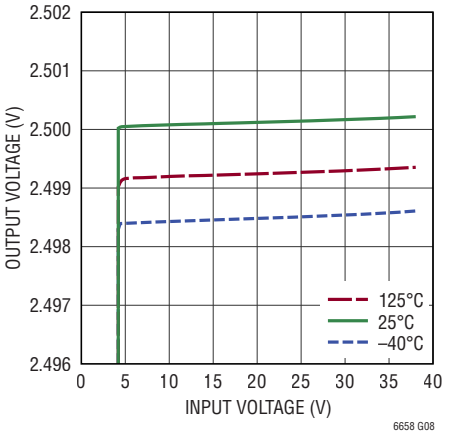
2.5V V_{OUT1} Load Regulation, Sinking



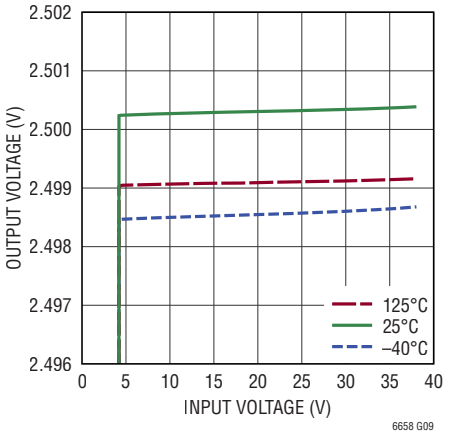
2.5V V_{OUT2} Load Regulation, Sinking



2.5V Line Regulation V_{OUT1}



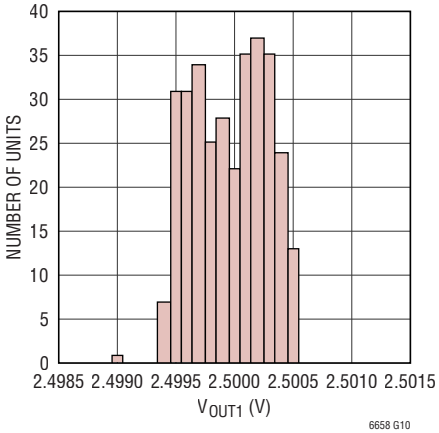
2.5V Line Regulation V_{OUT2}



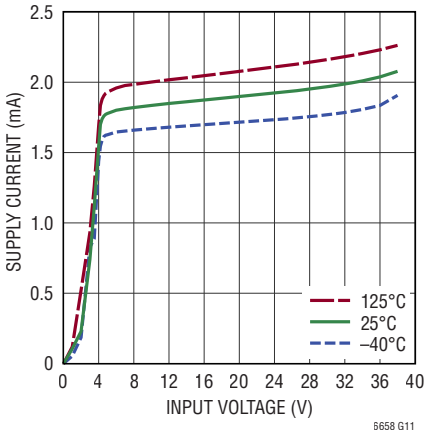
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{IN1} = V_{IN2} = V_{OUT1_F} + 2.5V = V_{OUT2_F} + 2.5V, C_{OUT1} = C_{OUT2} = 1µF, I_{LOAD} = 0mA, unless otherwise noted.

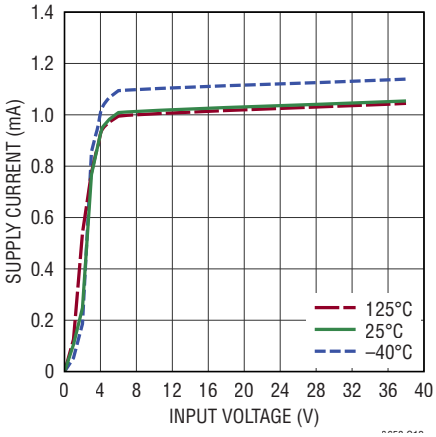
2.5V Output Accuracy Histogram



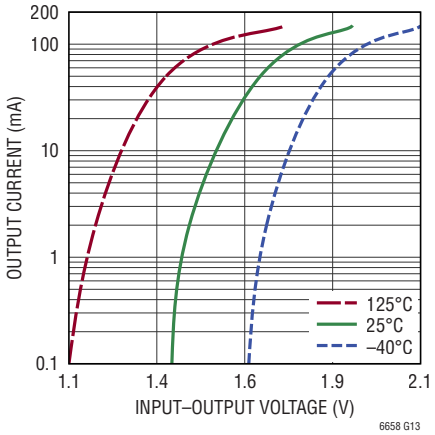
2.5V Supply Current vs Input Voltage



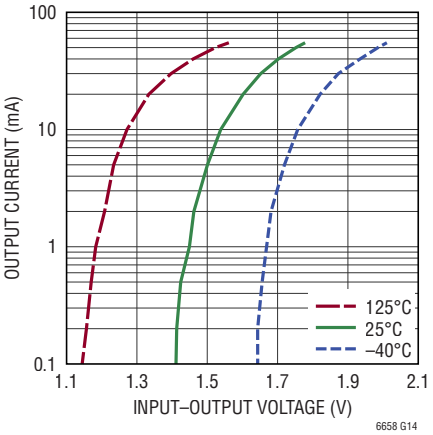
2.5V Output Disable ($\overline{OD}$) Low Supply Current vs Input Voltage



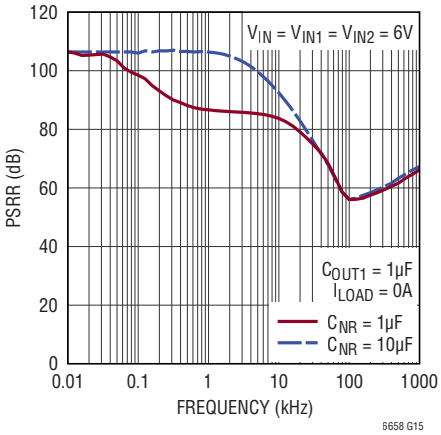
2.5V Minimum V_{IN} to V_{OUT1} Differential, Sourcing



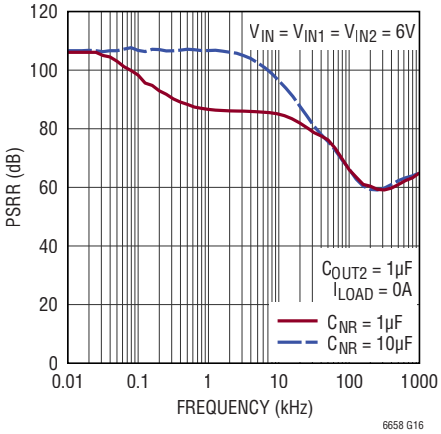
2.5V Minimum V_{IN} to V_{OUT2} Differential, Sourcing



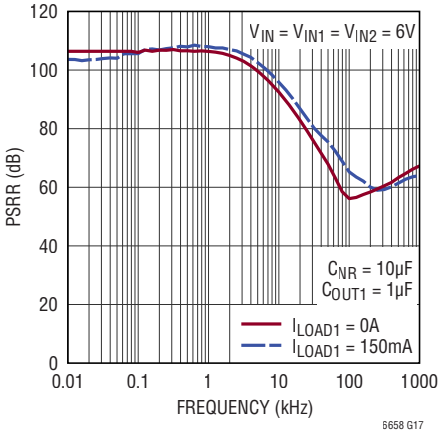
2.5V V_{OUT1} Power Supply Rejection Ratio vs Frequency



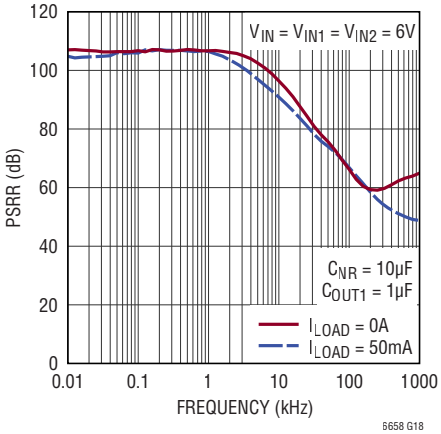
2.5V V_{OUT2} Power Supply Rejection Ratio vs Frequency



2.5V V_{OUT1} Power Supply Rejection Ratio vs Frequency



2.5V V_{OUT2} Power Supply Rejection Ratio vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

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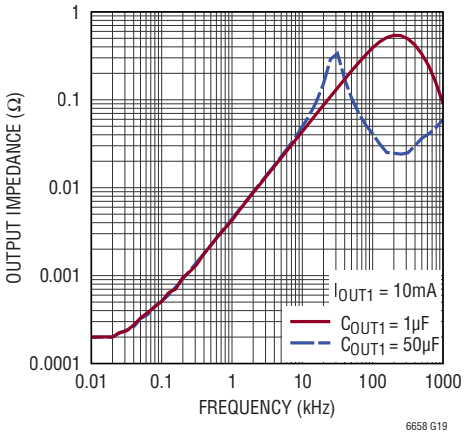
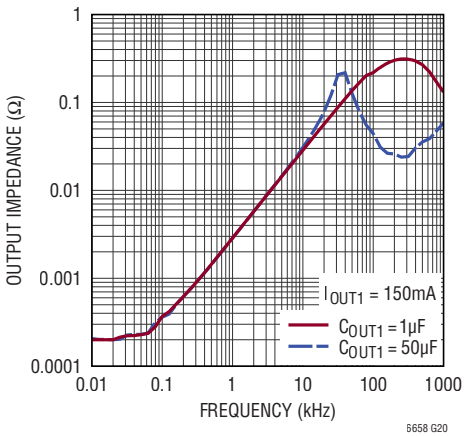
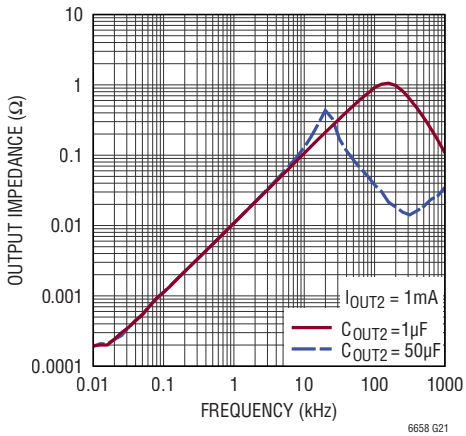
2.5V V_{OUT1} AC Output Impedance 10mA Load



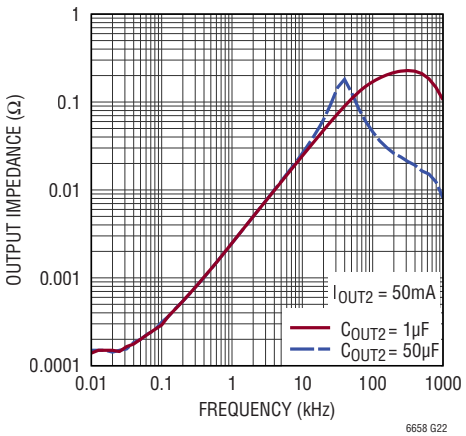
2.5V V_{OUT1} AC Output Impedance 150mA Load



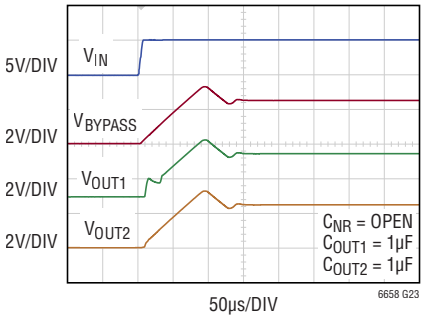
2.5V V_{OUT2} AC Output Impedance 1mA Load



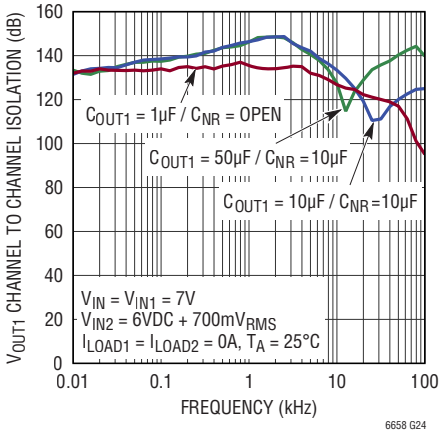
2.5V V_{OUT2} AC Output Impedance 50mA Load



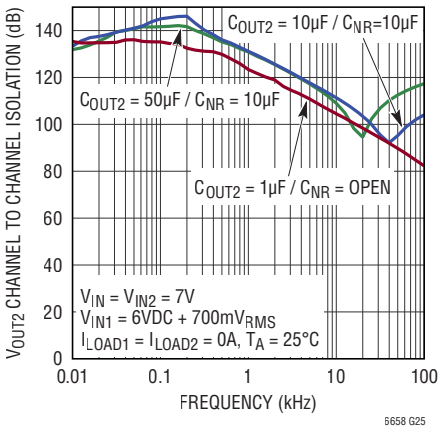
2.5V Turn-On Characteristic



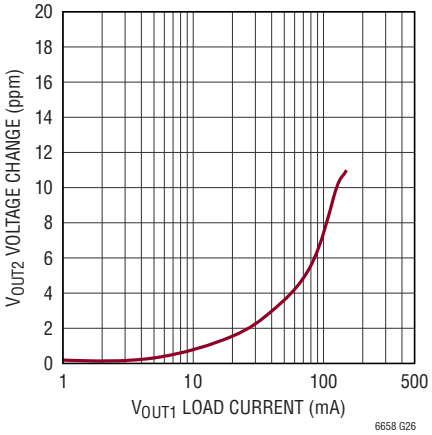
2.5V Channel to Channel Isolation V_{IN2} to V_{OUT1}



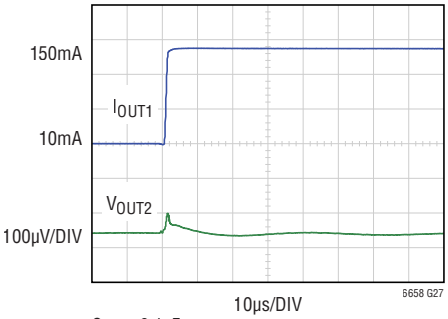
2.5V Channel to Channel Isolation V_{IN1} to V_{OUT2}



2.5V Channel to Channel Load Regulation (Effects of Heating Removed)



2.5V Channel to Channel Isolation, Time Domain

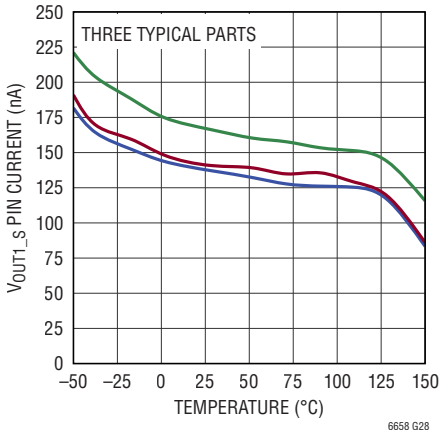


CNR = 0.1µF
COUT1 = 1µF
COUT2 = 1µF

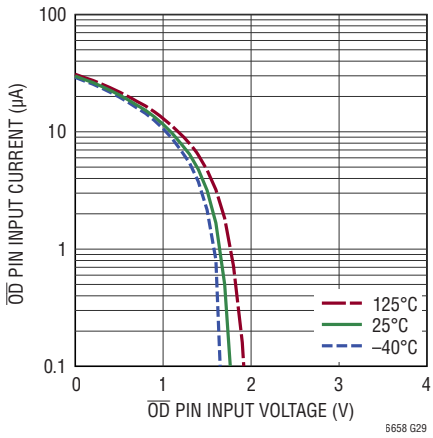
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{IN1} = V_{IN2} = V_{OUT1_F} + 2.5V = V_{OUT2_F} + 2.5V, C_{OUT1} = C_{OUT2} = 1µF, I_{LOAD} = 0mA, unless otherwise noted.

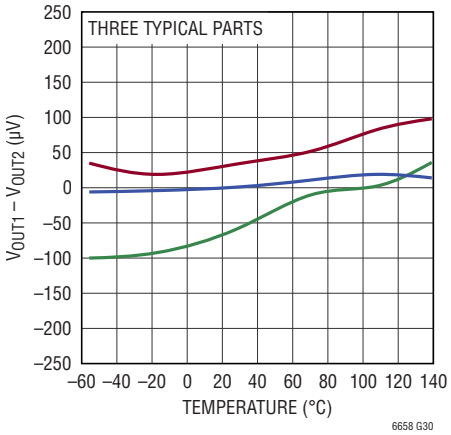
2.5V V_{OUT1_S} Pin Input Current vs Temperature



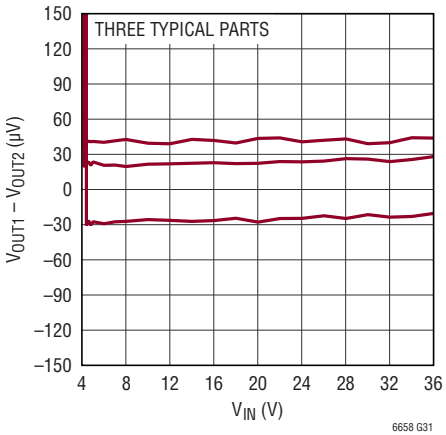
2.5V $\overline{OD}$ Pin Current vs $\overline{OD}$ Pin Input Voltage



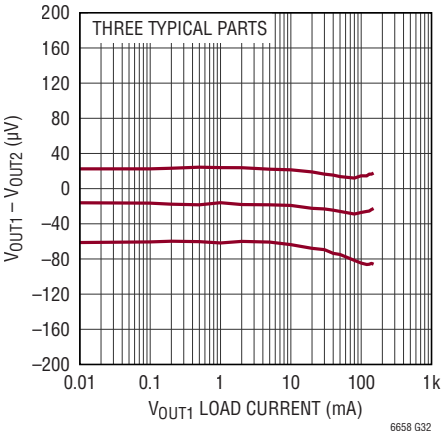
2.5V Tracking (V_{OUT1} – V_{OUT2}) vs Temperature



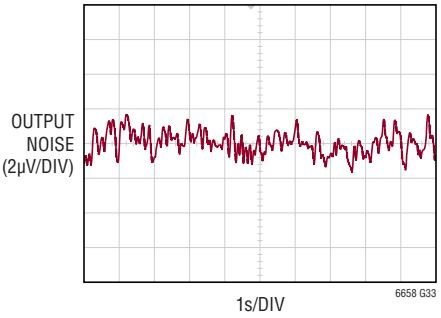
2.5V Tracking (V_{OUT1} – V_{OUT2}) vs Input Voltage



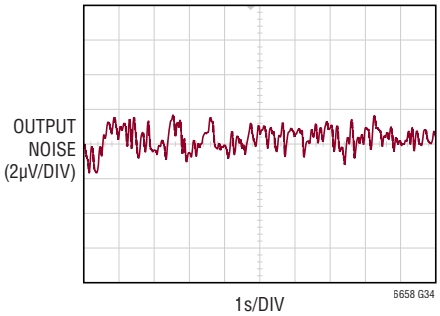
2.5V Tracking (V_{OUT1} – V_{OUT2}) vs V_{OUT1} Load Current



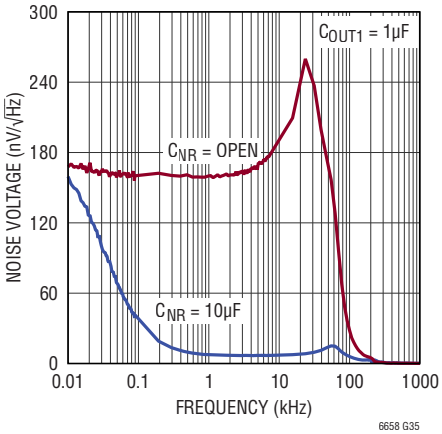
2.5V V_{OUT1} Output Noise 0.1Hz to 10Hz



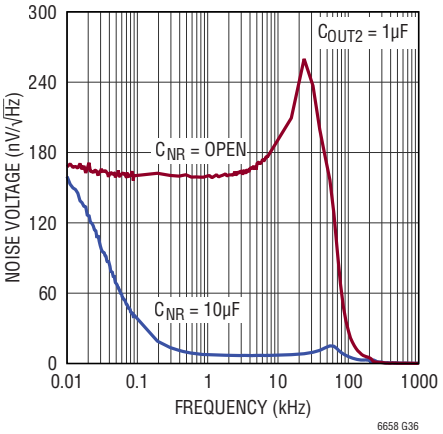
2.5V V_{OUT2} Output Noise 0.1Hz to 10Hz



2.5V V_{OUT1} Output Voltage Noise Spectrum I_{LOAD} = 0mA



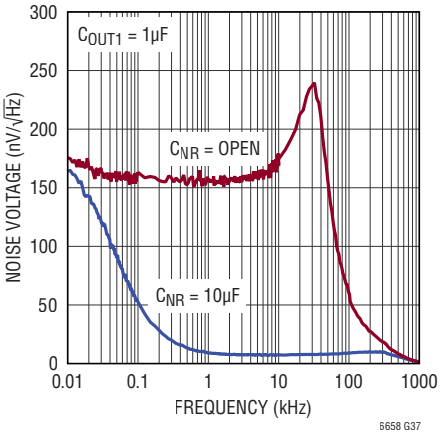
2.5V V_{OUT2} Output Voltage Noise Spectrum I_{LOAD} = 0mA



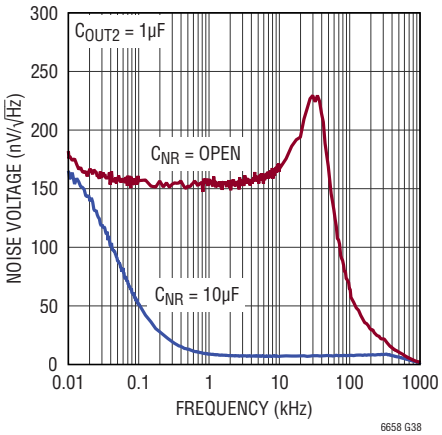
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{IN1} = V_{IN2} = V_{OUT1_F} + 2.5V = V_{OUT2_F} + 2.5V, C_{OUT1} = C_{OUT2} = 1µF, I_{LOAD} = 0mA, unless otherwise noted.

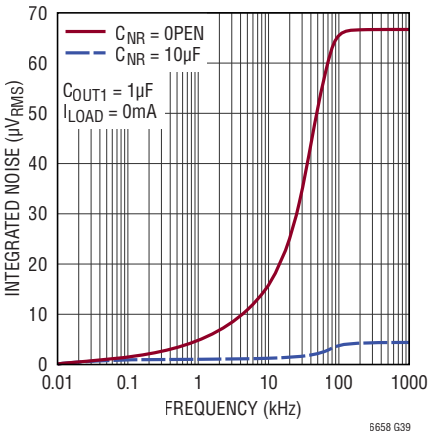
2.5V V_{OUT1} Output Voltage Noise Spectrum I_{LOAD} = 150mA



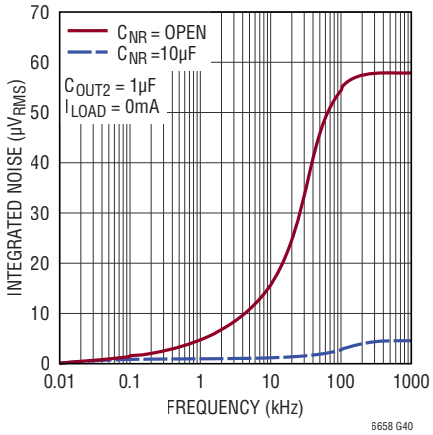
2.5V V_{OUT2} Output Voltage Noise Spectrum I_{LOAD} = 50mA



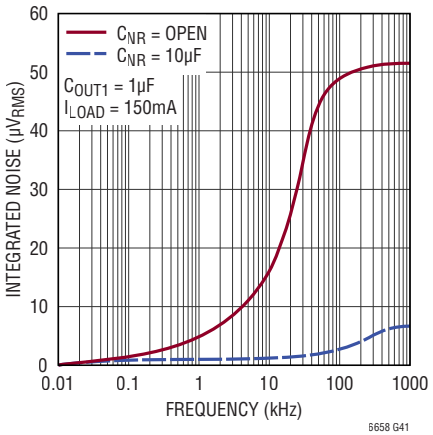
2.5V V_{OUT1} Integrated Noise I_{LOAD} = 0mA



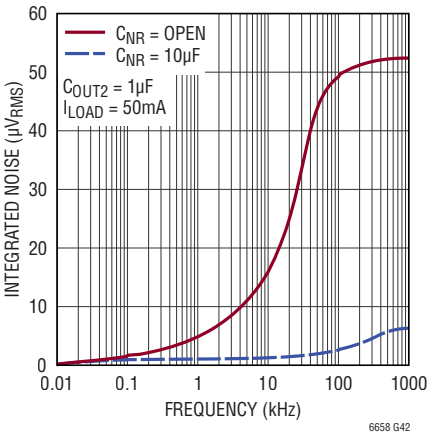
2.5V V_{OUT2} Integrated Noise I_{LOAD} = 0mA



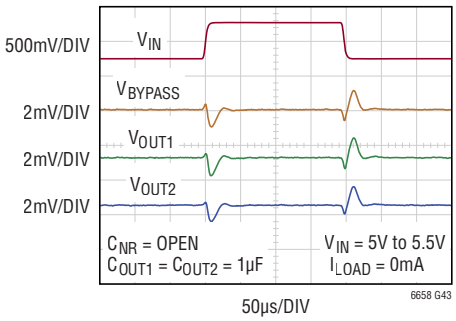
2.5V V_{OUT1} Integrated Noise I_{LOAD} = 150mA



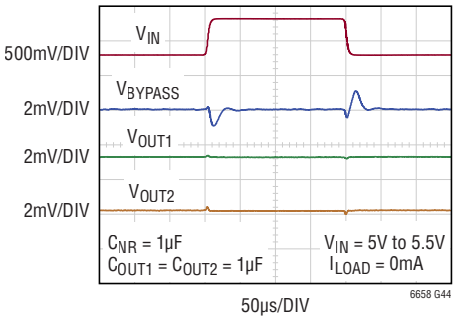
2.5V V_{OUT2} Integrated Noise I_{LOAD} = 50mA



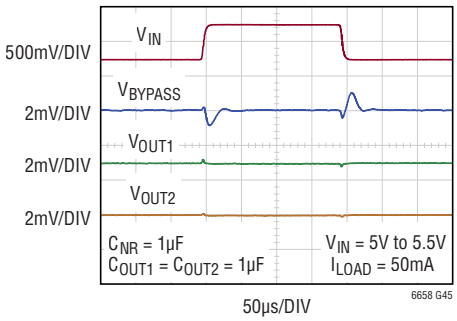
2.5V Line Transient Response



2.5V Line Transient Response



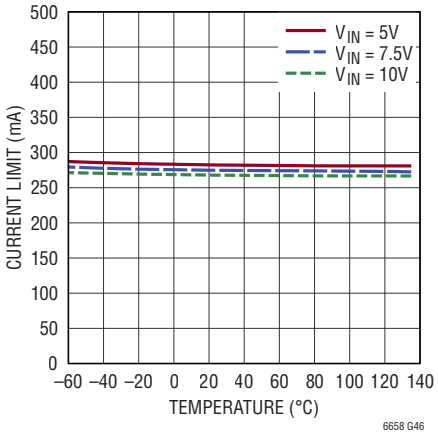
2.5V Line Transient Response



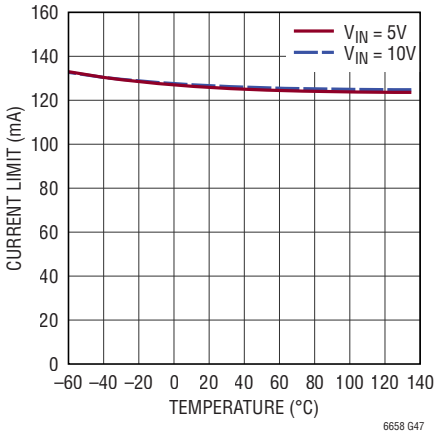
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = V_{IN1} = V_{IN2} = V_{OUT1_F} + 2.5V = V_{OUT2_F} + 2.5V, C_{OUT1} = C_{OUT2} = 1µF, I_{LOAD} = 0mA, unless otherwise noted.

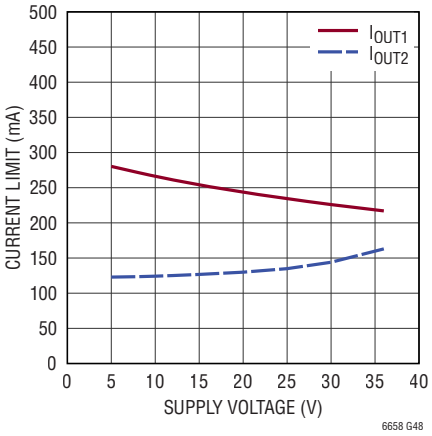
V_{OUT1} Current Limit



V_{OUT2} Current Limit



Current Limit vs Supply Voltage



PIN FUNCTIONS

GND (Pins 1, 2, 6, Exposed Pad Pin 17): These pins are the main ground connections and should be connected into a star ground or ground plane. The exposed pad must be soldered to ground for good electrical contact and rated thermal performance.

BYPASS (Pin 3): Bypass Pin. This requires a 1µF capacitor for bandgap stability.

DNC (Pin 4, 16): Do Not Connect. Keep leakage current from these pins to a minimum.

NR (Pin 5): Noise Reduction Pin. To band limit the noise of the reference, connect a capacitor between this pin and ground. See Applications Information section.

V_{OUT2_S} (Pin 7): V_{OUT2} Sense Pin. Connect this Kelvin sense pin at the load.

V_{OUT2_F} (Pin 8): V_{OUT2} Output Voltage. A 1µF to 50µF output capacitor is required for stable operation. This output can source up to 50mA.

$\overline{OD}$ (Pin 9): Output Disable. This active low input disables both outputs.

V_{IN2} (Pin 10): Input Voltage Supply for Channel 2. Bypass V_{IN2} with 0.1µF capacitor to ground. This pin supplies power to buffer amplifier 2.

V_{IN1} (Pin 11): Input Voltage Supply for Channel 1. Bypass V_{IN1} with 0.1µF capacitor to ground. This pin supplies power to buffer amplifier 1.

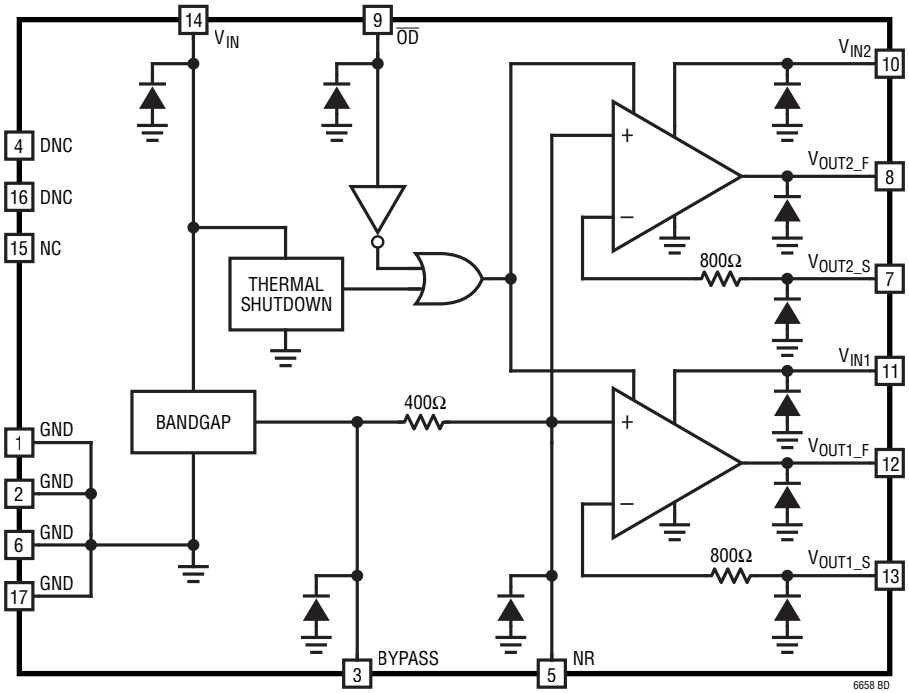
V_{OUT1_F} (Pin 12): V_{OUT1} Output Voltage. A 1µF to 50µF output capacitor is required for stable operation. This output can source up to 150mA.

V_{OUT1_S} (Pin 13): V_{OUT1} Sense Pin. Connect this Kelvin sense pin at the load.

V_{IN} (Pin 14): Input Voltage Supply. Bypass V_{IN} with 0.1µF capacitor to ground.

NC (Pin 15): No Connect.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT6658 combines the low noise and accuracy of a high performance reference and the high current drive of a regulator. The LT6658 is a high performance regulator providing two precise low noise outputs with Kelvin sense pins. The isolated outputs maintain their precision even when large voltage or current transients exist on the adjacent channel.

The LT6658 architecture consists of a low drift bandgap reference followed by an optional noise reduction stage and two independent buffers. The bandgap reference and the buffers are trimmed for low drift and high accuracy. The high gain buffers ensure outstanding line and load regulation.

The guidance that follows describes how to reduce noise, lower power consumption, generate different output voltages, and maintain low drift. Also included are notes on internal protection circuits, PCB layout, and expected performance.

Supply Pins and Ground

The LT6658 can operate with a supply voltage from V_{OUT} + 2.5V, to 36V. To provide design flexibility, the LT6658 includes 3 supply pins. The V_{IN} pin supplies power to the bandgap voltage reference. The V_{IN1} and V_{IN2} pins supply power to buffer amplifiers 1 and 2, respectively. Figure 1 illustrates how current flows independently through each of the output buffers. The simplest configuration is to connect all three supply pins together. To reduce power consumption or isolate the buffer amplifiers, separate the supply pins and drive them with independent supplies.

Separate V_{IN}, V_{IN1} and V_{IN2} supply pins isolate the bandgap reference and the two outputs V_{OUT1_F} and V_{OUT2_F} from each other. For example, a load current surge through V_{IN1} to V_{OUT1_F} is isolated from V_{OUT2_F} and the bandgap voltage reference. In Figure 2 a 140mA load current pulse on buffer 1 and the resulting output waveforms are shown. Despite the large current step on buffer 1, there is only a small transient at the output of buffer 2. When providing a stable voltage reference to quiet circuits like an ADC or DAC, it is important the two buffer outputs are isolated.

To minimize power consumption each supply pin can be operated with its minimum voltage. For example, if Buffer 1 has a 2.5V output, V_{IN1} can be operated at 5V. If Buffer 2's output is run at 3V, run V_{IN2} at 5.5V. The power savings gained by minimizing each supply voltage can be considerable.

Excessive ground current and parasitic resistance in ground lines can degrade load regulation. Unlike an LDO, the ground current of the LT6658 is designed such that ground current does not increase substantially when sourcing a large load current. All three ground pins and exposed pad should be connected together on the PCB, through a ground plane or through a separate trace terminating at a star ground.

The supply pins can be powered up in any order without an adverse response. However, all three supplies pins need the minimum specified voltage for proper operation.

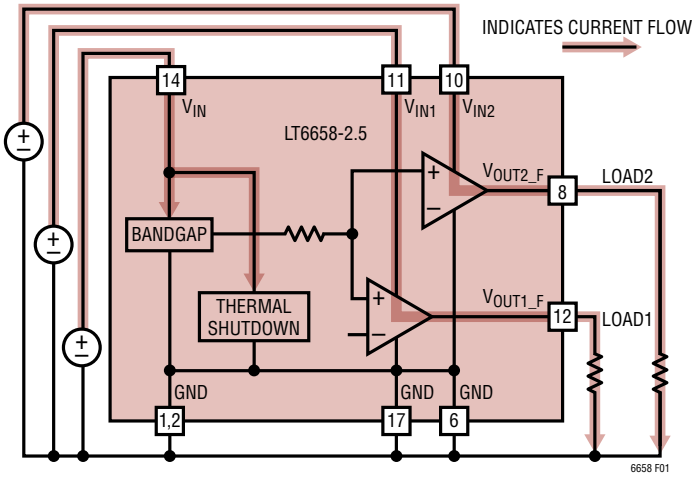


Figure 1. LT6658 Current Flow through the Supply Pins

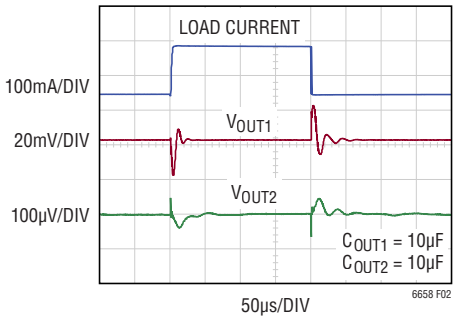


Figure 2. 10mA to 150mA Load Step on V_{OUT1}

APPLICATIONS INFORMATION

Input Bypass Capacitance

Each input voltage pin requires a 0.1µF capacitor located as close to the supply pin as possible. A 10µF capacitor is recommended for each supply where the supply enters the board. When the supply pins are connected together, a single 0.1µF and single 10µF capacitor can be used.

The BYPASS pin requires a 1µF capacitor for stability.

Stability and Output Capacitance

The LT6658 is designed to be stable for any output capacitance between 1µF and 50µF, under any load condition, specified input voltage, or specified temperature. Choosing a suitable capacitor is important in maintaining stability. Preferably a low ESR and ESL capacitor should be chosen. The value of the output capacitor will affect the settling response.

Care should be exercised in choosing an output capacitor, as some capacitors tend to deviate from their specified value as operating conditions change.

Although ceramic capacitors are small and inexpensive, they can vary considerably over the DC bias voltage. For example, the capacitance value of X5R and X7R capacitors will change significantly over their rated voltage range as shown in Figure 3. In this example the 1µF X5R capacitor loses almost 75% of its value at its rated voltage of 10V.

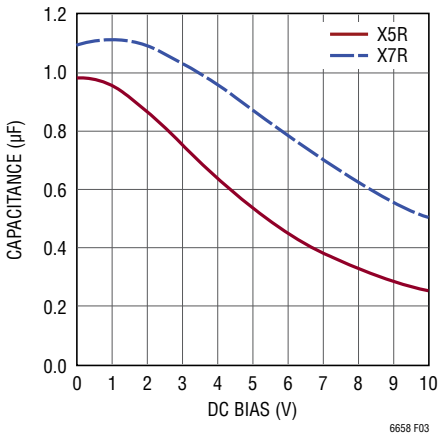


Figure 3. Capacitance Value of a 1µF X7R Over Its Full Rated Voltage

X5R and X7R capacitors will also vary up to 20% or more over a temperature range of –55°C to 125°C. This change in capacitance will be combined with any DC bias voltage variation.

Film capacitors do not vary much over temperature and DC bias as much as X5R and X7R capacitors, but generally they are only rated to 105°C. Film capacitors are also physically larger.

Effective series resistance (ESR) in the output capacitor can add a zero to the loop response of the output buffers creating an instability or excessive ringing. For the best results keep the ESR at or below 0.2Ω.

One measure of stability is the closed loop response of the output buffer. By driving the NR pin, a closed loop response can be obtained. In Figure 4 the closed loop response of the output buffer with three different output capacitance values is shown. In the Figure 5 the same plot is repeated with a 150mA load.

A large value electrolytic capacitor with a 1µF to 50µF ceramic capacitor in parallel can be used on the output pins. The buffers will be stable, and the bandwidth will be lower.

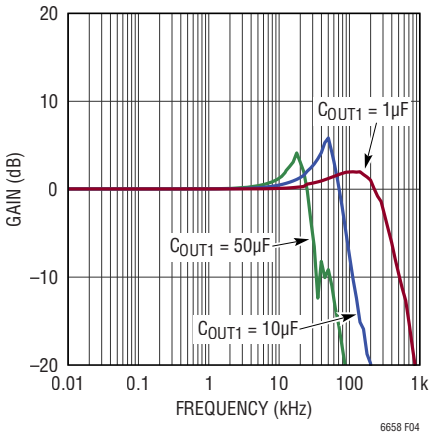


Figure 4. LT6658 Closed Loop Response of the Channel 1 Output Buffer for 3 Values of Output Capacitance and No Load

APPLICATIONS INFORMATION

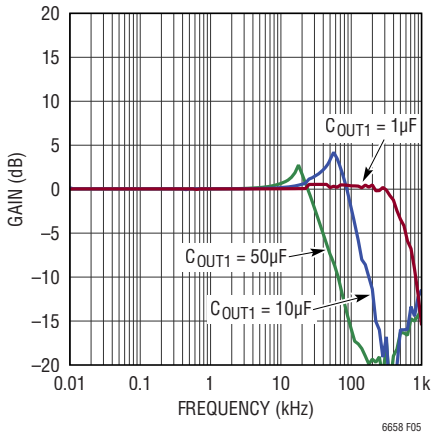


Figure 5. LT6658 Closed Loop Response of the Channel 1 Output Buffer for 3 Values of Output Capacitance and 150mA Load

The Channel 2 output buffer has a similar response.

Start-Up and Transient Response

When the LT6658 is powered up, the bandgap reference charges the capacitor on the BYPASS pin. The output buffer follows the voltage on the BYPASS pin charging the output capacitor. Figure 6 shows the start-up response on the BYPASS and V_{OUT1_F} pins for three different output capacitor values. The start-up response is limited by the current limit in the bandgap charging the BYPASS capacitor. The turn-on time is also restricted by the current limit in the output buffer and the size of the output capacitor. A larger output capacitor will take longer to charge. Adding a capacitor to the NR pin will also affect turn-on time.

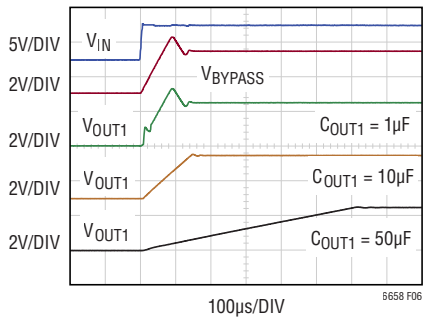


Figure 6. Start-Up Response on the BYPASS and V_{OUT1_F} Pins

The test circuit for the transient response test is shown in Figure 7. The transient response due to load current steps are shown in Figures 8, 9, and 10.

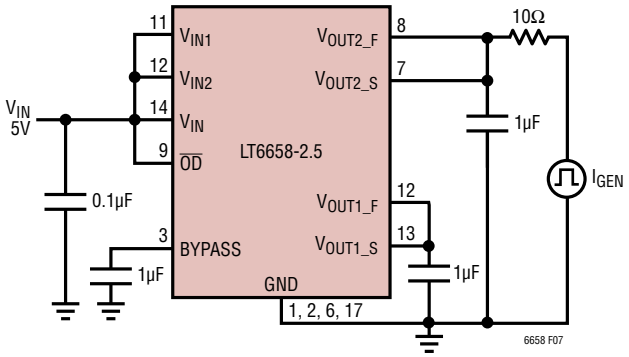


Figure 7. Load Current Response Time Test Circuit

In Figure 8 and Figure 9, a 75mA and 140mA load step is applied to Channel 1, respectively. In Figure 10, a 40mA load step is applied to Channel 2. The settling time is determined by the size and edge rate of the load step, and the size of the output capacitor.

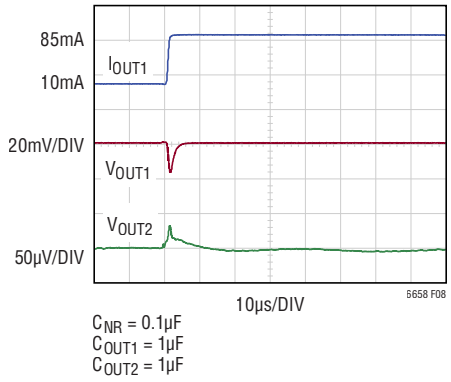


Figure 8. LT6658-2.5 Output 1 Response to 75mA Load Step

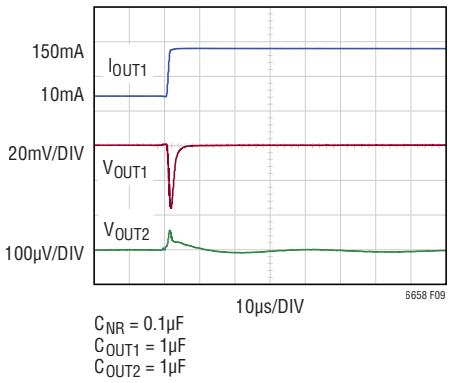


Figure 9. LT6658-2.5 Output 1 Response to 140mA Load Step

APPLICATIONS INFORMATION

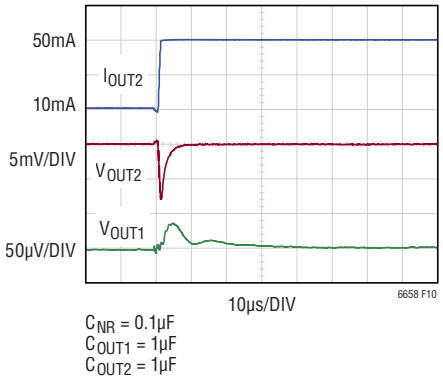


Figure 10. LT6658-2.5 Output 2 Response to 40mA Load Step

Output Voltage Scaling

Each output can be configured with external resistors to gain up V_{OUT}, enabling the output to be set from 2.5V to 6V. Unity gain is configured by tying the sense and force pins together.

In Figure 11, Channel 2 is configured with a gain of 2 (see Typical Applications Section for more examples). This can be done to one or both of the channels. When configuring a gain >1 make sure that the associated supply pin is 2.5V higher than the V_{OUT_F} pin. Also note that the absolute maximum voltage on the output pins (both force and sense) is 6V. Place the gain resistors close to the part keeping the traces short. Since this is part of the feedback path, the feedback resistor should be connected near the load, avoiding any resistive parasitic in the high current path. Another source of error is having some resistance in the feedback network to ground. If possible the resistor should be connected as close as possible to the chip ground.

When using non-unity gain configurations, V_{OS} drift errors are possible. There is an 800Ω resistor in the Kelvin sense line which is designed to cancel base current variation on the input of the buffer amplifier. Matching the impedances on the positive and negative inputs reduces base current error and minimizes V_{OS} drift. A feedback network will have a small base current flowing through the feedback resistor possibly causing a small V_{OS} drift.

Referring to the 2.5V V_{OUT1_S} Pin Input Current vs Temperature plot in the Typical Performance Characteristics section, the input sense current varies about 50nA between –40°C and 125°C. This 50nA variation may cause a 0.5mV voltage change across the 10kΩ feedback resistor affecting the output voltage.

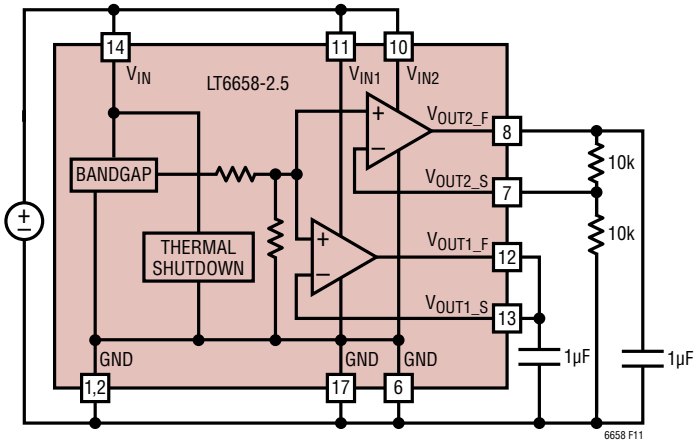


Figure 11. The LT6658-2.5 with Output 2 Configured for a 5V Output

Kelvin Sense Pins

To ensure the LT6658 maintains good load regulation, the Kelvin sense pins should be connected close to the load to avoid any voltage drop in the copper trace on the force pin. It only takes 10mΩ of resistance to develop a 1.5mV drop with 150mA. This would cause an ideal 2.5V output voltage to exceed the 0.05% specification at the load. The circuit in Figure 12a illustrates how an incorrect Kelvin sense connection can lead to errors. The parasitic resistance of the copper trace will cause the output voltage to change as the load current changes. As a result, the voltage at the load will be lower than the voltage at the sense line. The circuit in Figure 12b shows the proper way to make a Kelvin connection with the sense line as close to the load as possible. The voltage at the load will now be well regulated. The V_{OUT1_S} current is typically 135nA, and a low resistance in series with the Kelvin sense input is unlikely to cause a significant error or drift.

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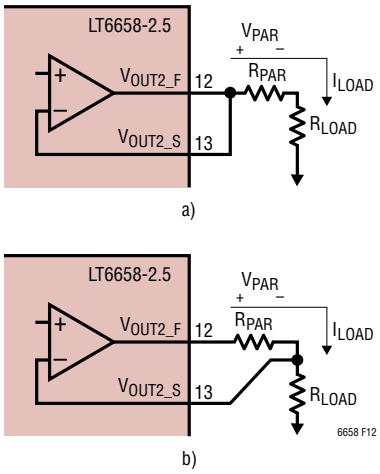

Figure 12. How to Make a Proper Kelvin Sense Connection

Output Noise and Noise Reduction (NR)

The LT6658 noise characteristic is similar to that of a high performance reference. The total noise is a combination of the bandgap noise and the noise of the buffer amplifier. The bandgap noise can be measured at the NR pin and is shown in Figure 13 with a 1µF capacitor, 10µF capacitor and no capacitor on the NR pin. The bandgap can be bandlimited by connecting a capacitor between the NR pin and ground. The RC product sets the low pass 3dB corner attenuating the out-of-band noise of the bandgap. An internal 400Ω ±15% resistor combines with the external capacitor to create a single-pole low pass filter. Table 1 lists capacitor values and the corresponding 3dB cutoff frequency.

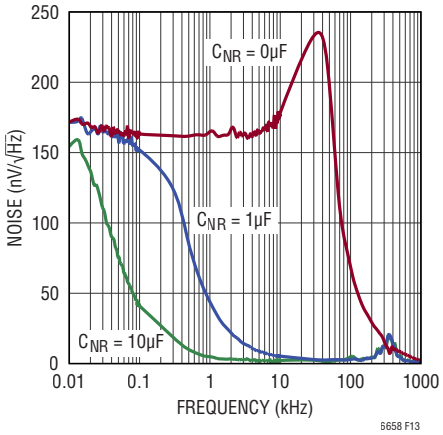

Figure 13. LT6658 Bandgap Output Voltage Noise

Table 1. NR Capacitor Values and the Corresponding 3dB Frequency

NR Capacitor (µF)	NR 3dB Frequency (Hz)
0.1	3979
0.22	1809
0.47	847
1	398
2.2	181
4.7	85
10	40
22	18

The primary trade-off for including an RC filter on the NR pin is a slower turn-on time. The effective resistance seen by the NR capacitor is 400Ω. The RC time constant (τ) for charging the NR capacitor is $\tau = R \bullet C$. To reach the initial accuracy specification for the LT6658, 0.05%, it will take 7.6τ of settling time. Example settling time constants are shown in Table 2. An example of the NR pin charging and the relationship to the output voltage is shown in Figure 14. The appropriate trade-off between settling time and noise limiting is specific to the demands of each unique application.

Table 2. Settling Times for Different NR Capacitor Values

Output Voltage (V)	NR Pin Resistance (Ω)	C (µF)	7.6τ (ms)
2.5	400	0.01	0.030
		0.1	0.30
		1	3.04

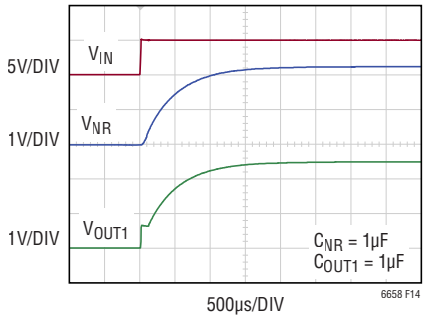

Figure 14. Start-up Response on the NR pin and V_{OUT_F}

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The LT6658's two low noise buffer amplifiers measure 8nV/√Hz. The combined bandgap and buffer noise results for Buffer 1 and Buffer 2 are shown in the Typical Performance Characteristics section. Note that beyond the NR pin cutoff frequency, the noise is primarily due to the buffer amplifiers. As shown, the buffer can be bandlimited by increasing the size of the output capacitors. Figure 15 and Figure 16 show the total integrated noise of Buffer 1 and Buffer 2, respectively.

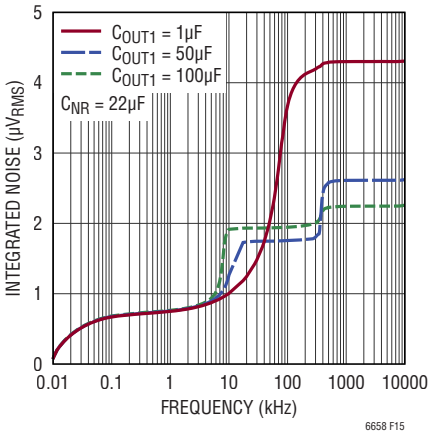

Figure 15. LT6658-2.5 Total Integrated Output Voltage Noise with C_{NR} = 22µF and C_{OUT1} = 1µF, 50µF and 100µF Output Capacitors

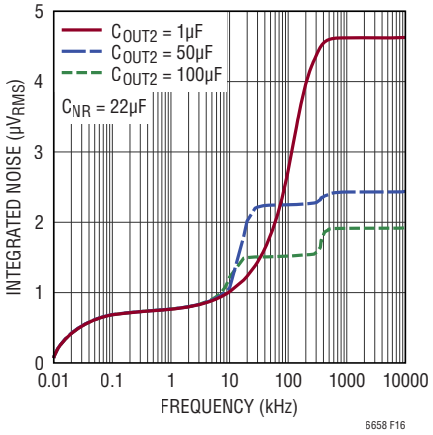

Figure 16. LT6658-2.5 V_{OUT2} Integrated Noise with C_{NR} = 22µF and C_{OUT2} = 1µF, 50µF and 100µF

The output voltage noise does not change appreciably as load current increases.

The wide range of output capacitance capability and the NR pin capacitance allows the LT6658 noise density spectrum to be customized for specific applications. Table 3 lists the output noise for different conditions.

The output and NR capacitances also affect the AC PSRR response as shown in Table 3. See the Typical Performance Characteristics section for more information.

Table 3. Output Noise and Ripple Rejection Typical Values

PARAMETER	CONDITIONS	TYP	UNITS
Output Noise Voltage (V_{OUT1} and V_{OUT2})	Frequency = 10Hz, C_{OUT} = 1µF, C_{NR} = 0F, I_{LOAD} = Full Current*	176	nV/√Hz
	Frequency = 10Hz, C_{OUT} = 1µF, C_{NR} = 10µF, I_{LOAD} = Full Current*	164	nV/√Hz
	Frequency = 1kHz, C_{OUT} = 1µF, C_{NR} = 0F, I_{LOAD} = Full Current*	157	nV/√Hz
	Frequency = 1kHz, C_{OUT} = 1µF, C_{NR} = 10F, I_{LOAD} = Full Current*	9	nV/√Hz
Output RMS Noise	10Hz to 100kHz, C_{OUT1} = 1µF, C_{NR} = 0F	26.2	ppm_{RMS}
	10Hz to 100kHz, C_{OUT1} = 1µF, C_{NR} = 10µF	1.5	ppm_{RMS}
	10Hz to 100kHz, C_{OUT1} = 50µF, C_{NR} = 22µF	0.7	ppm_{RMS}
	10Hz to 100kHz, C_{OUT2} = 1µF, C_{NR} = 0F	21.8	ppm_{RMS}
	10Hz to 100kHz, C_{OUT2} = 1µF, C_{NR} = 10µF	1.1	ppm_{RMS}
	10Hz to 100kHz, C_{OUT2} = 50µF, C_{NR} = 22µF	0.9	ppm_{RMS}
Power Supply Rejection (V_{IN1} = V_{OUT1} + 3V, V_{IN2} = V_{OUT2} + 3V)	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD1} = 150mA, C_{OUT1} = 1µF, C_{NR} = 1µF	107	dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD1} = 150mA, C_{OUT1} = 1µF, C_{NR} = 1µF	96	dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD1} = 150mA, C_{OUT1} = 1µF, C_{NR} = 1µF	65	dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD1} = 150mA, C_{OUT1} = 1µF, C_{NR} = 1µF	64	dB
	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD2} = 50mA, C_{OUT2} = 1µF, C_{NR} = 1µF	104	dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD2} = 50mA, C_{OUT2} = 1µF, C_{NR} = 1µF	96	dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_{LOAD2} = 50mA, C_{OUT2} = 1µF, C_{NR} = 1µF	66	dB
	V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD2} = 50mA, C_{OUT2} = 1µF, C_{NR} = 1µF	65	dB

* The full current for I_{LOAD} is 150mA and 50mA for output 1 and output 2, respectively.

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Power Supply Rejection

The three supply pins provide flexibility depending on the demands of the application. The LT6658 provides excellent AC power supply rejection with all three supply pins connected together. Superior performance can be achieved when the supply pins are independently powered. For example, use a quiet supply for the V_{IN} pin. This will isolate the bandgap circuit from the outputs. Further, each buffer can be supplied independently providing >140dB of isolation across some frequencies. Table 3 summarizes several conditions of power supply rejection.

Output Disable

The $\overline{OD}$ pin disables the output stage of both output buffers. This pin is useful for disabling the buffers when fault conditions exist. For example, if external circuitry senses that the load is too hot or there is a short circuit condition, asserting this pin will remove the output current. This active low pin will disable the output buffers when the voltage on the pin is less than 0.8V. When the input voltage is greater than 2V the LT6658 is enabled.

The start-up time when the LT6658 enables is determined by the size of the output capacitor. Figure 17 is an example of the LT6658-2.5 being enabled and disabled. The $\overline{OD}$ pin has an internal pull-up current that will keep the output buffers enabled when the $\overline{OD}$ pin floats. In noisy environments, it is recommended that $\overline{OD}$ be tied high explicitly.

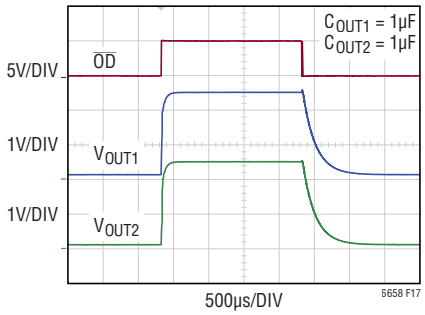

Figure 17. The Output Disable Function

Internal Protection

There are two internal protection circuits for monitoring output current and die temperature.

The output stage of each output buffer is disabled when the internal die temperature is greater than 165°C. There is 11°C of hysteresis allowing the part to return to normal operation once the die temperature drops below 154°C.

In addition, a short circuit protection feature prevents the output from supplying an unlimited load current. A fault or short on either output force pin will cause the output stage to limit the current and the output voltage will drop accordingly to the output fault condition. For example, if a 1Ω fault to ground occurs on Channel 1, the circuit protection will limit both outputs. A load fault on either channel will affect the output of both channels.

Power Dissipation

To maintain reliable precise and accurate performance the LT6658 junction temperature should never exceed T_{JMAX} = 150°C. If the part is operated at the absolute maximum input voltage and maximum output currents, the MSE package will need to dissipate over 7 watts of power.

The LT6658 is packaged in an MSE package with an exposed pad. The thermal resistance junction to case, θ_{JC}, of the MSE package is 10°C/W. The thermal resistance junction to ambient, θ_{JA}, is determined by the amount of copper on the PCB that is soldered to the exposed pad. When following established layout guidelines the θ_{JA} can be as low as 35°C/W for the MSE package.

As a simple example, if 2 watts is dissipated in the MSE package, the die temperature would rise 70°C above the ambient temperature. The following expression describes the rise in temperature ($\theta_{JA} \bullet P_{TOTAL}$), and the increase of junction temperature over ambient temperature as

$$T_J = T_A + \theta_{JA} \bullet P_{TOTAL}$$

where T_J is the junction temperature, T_A is the ambient temperature, θ_{JA} is the thermal resistance junction to ambient, and P_{TOTAL} is the total power dissipated in the LT6658. Further, if the package was initially at room temperature (25°C), the die would increase to 95°C. At 3 watts the die would exceed the specified H-grade temperature of 125°C.

The derating curve for the MSE package is shown in Figure 18. Three different θ_{JA} curves are shown. θ_{JA} is dependent on the amount of copper soldered to the

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exposed pad. Multiple layers of copper with multiple vias is recommended.

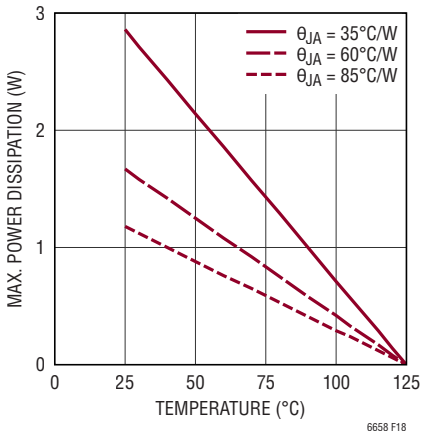

Figure 18. MSE Derating Curve

The power dissipated by the LT6658 can be calculated as three components. There is the power dissipated in the two output devices (one for each channel) and the power dissipated within the remaining internal circuits. Calculate the power in the remaining circuits using the following expressions

$$P_{STATIC} = V_{IN} \bullet I_{STATIC}$$

where P_{STATIC} is the power dissipated in the LT6658 minus the output devices, V_{IN} is the supply voltage, and I_{STATIC} is the current flowing through the LT6658. To calculate the power dissipated by the output devices use

$$P1 = (V_{IN1} - V_{OUT1}) \bullet I_{OUT1}$$

$$P2 = (V_{IN2} - V_{OUT2}) \bullet I_{OUT2}$$

where P1 and P2 are the power dissipated in the Channel 1 and Channel 2 output devices, V_{IN1} and V_{IN2} are the supply voltages for each channel, and V_{OUT1} and V_{OUT2} are the output voltages. Finally,

$$P_{TOTAL} = P1 + P2 + P_{STATIC}$$

where P_{TOTAL} is the total power dissipated in the package. P_{STATIC} tends to be much smaller than P1 or P2.

To lower the power in the output devices, the supply voltage for each of the output buffers can be reduced to only 2.5V above the output voltage. For example, with a 2.5V output, use a 5V supply and maximum output current on each channel, the total power can be calculated as

$$P1 = (5V - 2.5V) \bullet 0.15A = 0.375W$$

$$P2 = (5V - 2.5V) \bullet 0.05A = 0.125W$$

$$P_{STATIC} = 5V \bullet 0.001A = 0.005W$$

$$P_{TOTAL} = 0.375W + 0.125W + 0.005W = 0.505W$$

which is an operating condition that can be tolerated above 100°C when proper heat sinking is used.

In Figure 19, the output current in both channels is increased linearly for three values of V_{IN} where all three supply pins are connected together. As V_{IN} and I_{OUT} increases, the total power increases proportionally. When the supply voltage is 30V and the total output current is 200mA, the power exceeds 5W, representing a junction temperature increase of over 175°C using a best case scenario when using a MSE with a θ_{JA} = 35°C/W. Figure 20, illustrates how rapidly power increases when the supply voltage increases, especially with 200mA of total load current. If possible, reduce the voltage on V_{IN1} and V_{IN2}, which in turn will reduce the power dissipated in the LT6658 package.

The LT6658 is a high performance reference and extreme thermal cycling will cause thermal hysteresis and should be avoided if possible. See the Thermal Hysteresis section.

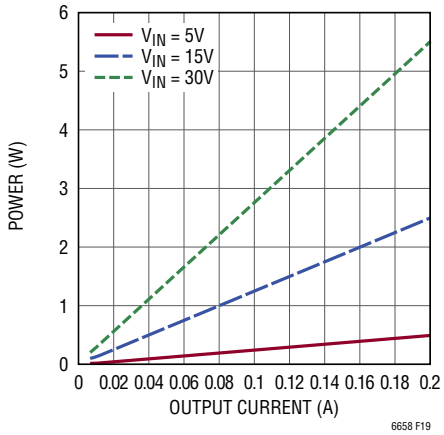

Figure 19. Power Dissipation vs Output Current

When the supply voltage, V_{IN1} or V_{IN2}, is greater than 30V, a hard short from either output to ground can result in more than 3 to 6 watts of instantaneous power which can damage the output devices.

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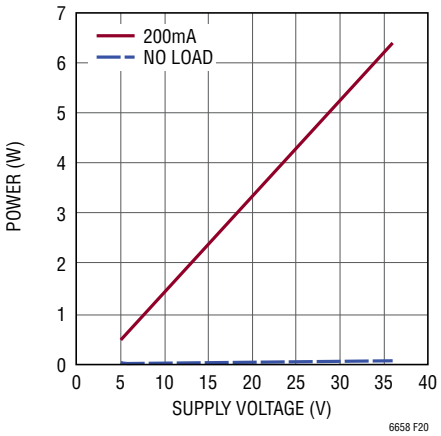

Figure 20. Power Dissipation vs Supply Voltage

Safe Operating Area

The safe operating area, or SOA, describes the operating region where the junction temperature does not exceed T_{JMAX}. In Figure 21, the SOA for the LT6658 is plotted. In this plot, the output voltage is 2.5V and the output current is the combined current of both channels. The SOA is plotted for three values of θ_{JA}. This illustrates how a lower θ_{JA} value will remove more heat and allow more power to be dissipated through the package without damaging the part.

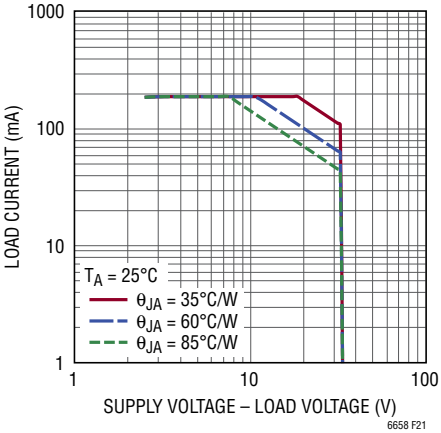

Figure 21. SOA for the LT6658

There are three regions in the SOA plot. The top left region is the maximum rated current of the LT6658. The diagonal lines in the middle are where both the load current and supply voltage must be reduced as not to exceed T_{JMAX}. The bottom right is the maximum voltage of the LT6658.

It is important to realize the SOA limit is an absolute maximum rating at T_{JMAX}. It is not recommended to operate at this limit for extended periods of time.

PCB Layout

The LT6658 is a high performance reference and therefore, requires good layout practices. Each supply pin should have 0.1µF capacitor placed close to the package. The output capacitors should also be close to the part to keep the equivalent series resistance to a minimum. As mentioned earlier, avoid parasitic resistance between the sense line and the load. Any error here will directly affect the output voltage.

All three ground pins (1, 2, 6) , and exposed pad should be connected together, preferably in a star ground configuration or ground plane. The exposed pad, Pin 17, is electrically connected to the die and must be connected to ground. It is also necessary for good thermal conductivity to use plenty of copper and multiple vias.

If the design requires the part to dissipate significant power, consider using 2oz copper and/or a multilayer board with a large area of copper connected to the exposed pad. Note that θ_{JA} is proportional to the amount of copper soldered to the exposed pad. Preferably the copper should be on the outermost layers of the board for good thermal dissipation. A sample layout is shown in Figure 22a. The sense lines, V_{OUT1_S} and V_{OUT2_S} should connect as close as possible to the top of the load. In Figure 22b, a star ground is shown where the LT6658 ground is directly connected to the bottom of the load. Connect all other grounds in the system to this same point. Minimize the resistance between GND side of the load and the LT6658 GND pins, especially for applications where the LT6658 is sinking current. This minimizes load regulation errors.

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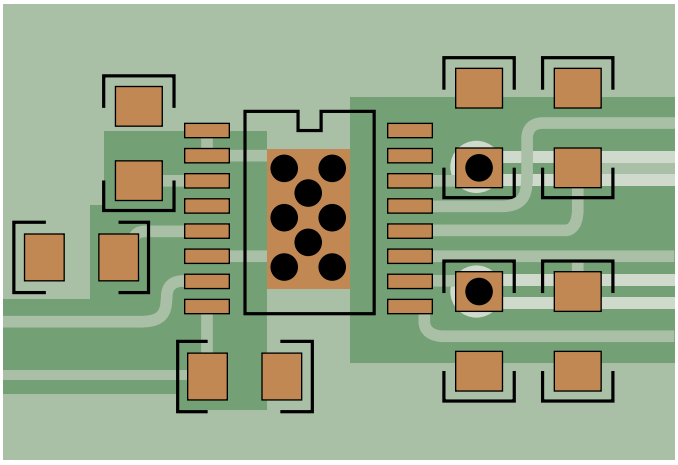
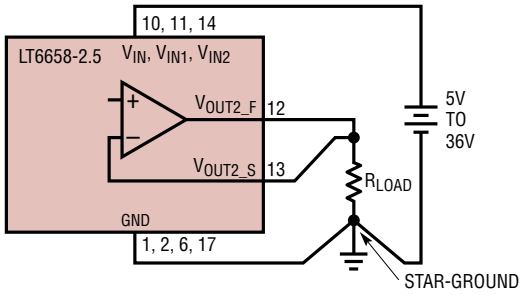


(a) LT6658 Sample PCB Layout



(b) Bring Out Ground to the Load and Make a Star Connection

Figure 22.

Long Term Drift

Long term drift is a settling of the output voltage while the part is powered up. The output slowly drifts at levels of parts per million (ppm). The first 1000 hours of being powered up sees the most shift. By the end of 3000 hours, most parts have settled and will not shift appreciably. The plot in Figure 23 is representative of the LT6658 long term drift.

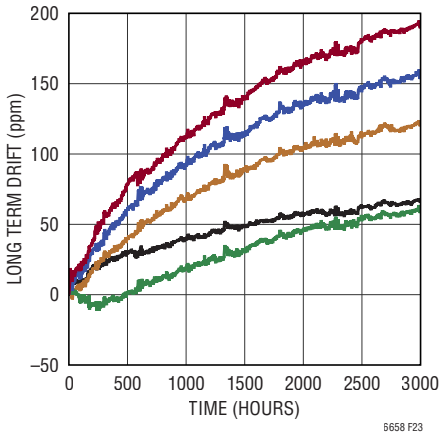


Figure 23. LT6658 Long Term Drift

IR Reflow Shift

As with many precision devices, the LT6658 will experience an output shift when soldered to a PCB. This shift is caused by uneven contraction and expansion of the plastic mold compound against the die and the copper pad underneath the die. Critical devices in the circuit will experience a change of physical force or pressure, which in turn changes its electrical characteristics, resulting in subtle changes in circuit behavior. Lead free solder reflow profiles reach over 250°C, which is considerably higher than lead based solder. A typical lead free IR reflow profile is shown in Figure 24. The experimental results simulating this shift are shown in Figure 25. In this experiment, LT6658 is run through an IR reflow oven once and three times.

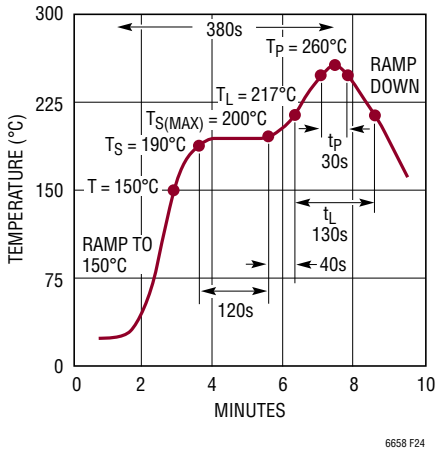


Figure 24. Lead Free Reflow Profile

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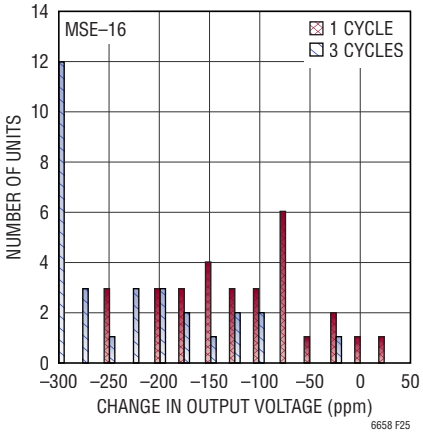
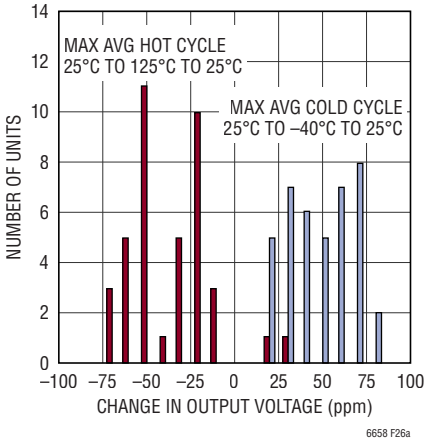


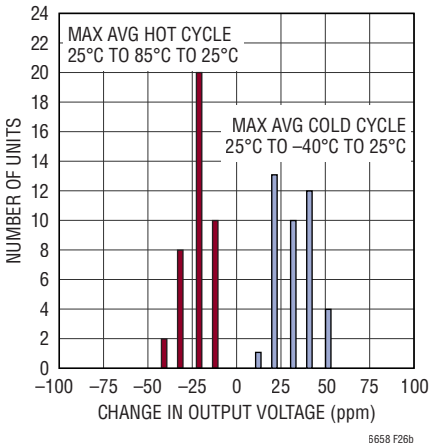
Figure 25. ΔV_{OUT1} Due to IR Reflow Shift

Thermal Hysteresis

Thermal hysteresis is caused by the same effect as IR reflow shift. However, in the case of thermal hysteresis, the temperature is cycled between its specified operating extremes to simulate how the part will behave as it experiences extreme temperature excursions and then returns to room temperature. For example, an H-grade part is repeatedly cycled between 125°C and –40°C. Each time the temperature passes through 25°C, the output voltage is recorded. The plots in Figure 26 illustrate the change in output voltage from the initial output voltage after a cold and hot excursion.



(a) H-Grade

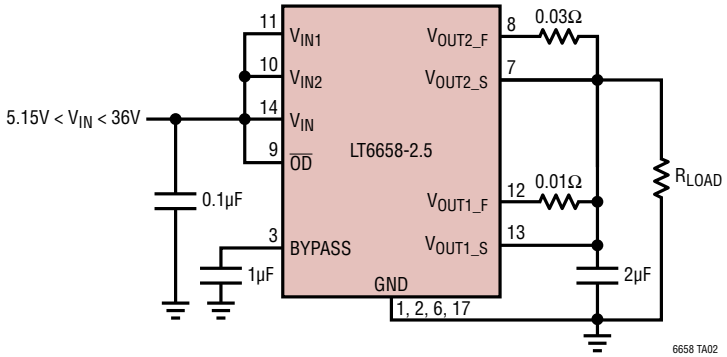


(b) I-Grade

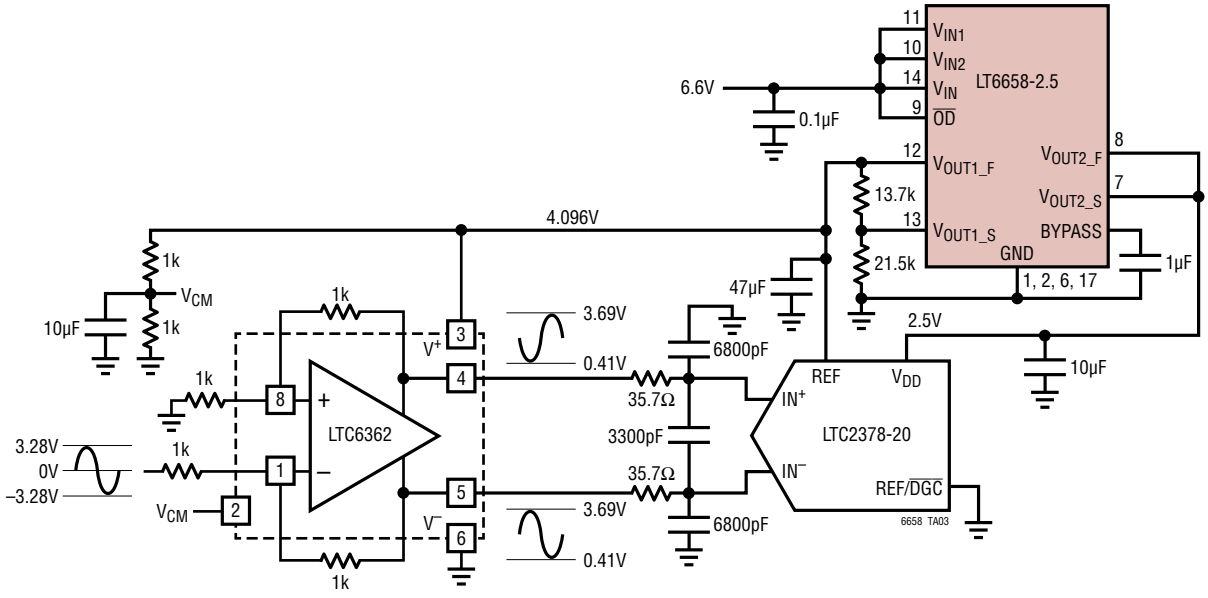
Figure 26. Thermal Hysteresis

TYPICAL APPLICATIONS

200mA Reference

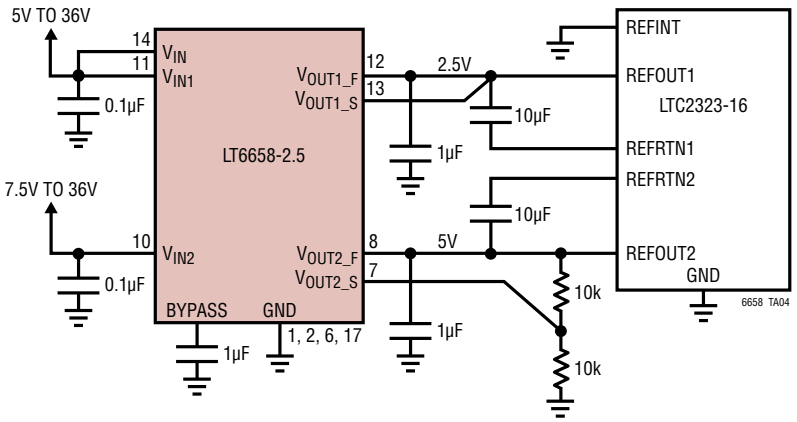


Single Supply Precision Data Acquisition Circuit

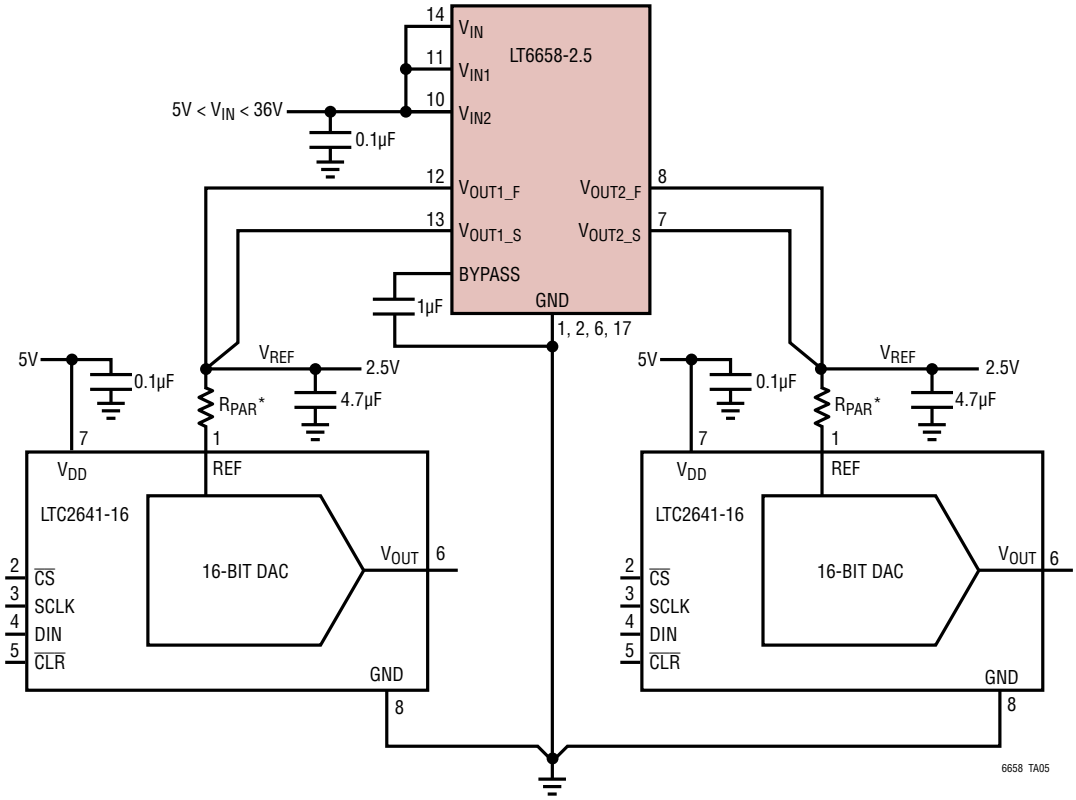


TYPICAL APPLICATIONS

LT6658 Driving the LTC2323-16 Dual ADC with Independent Voltage References



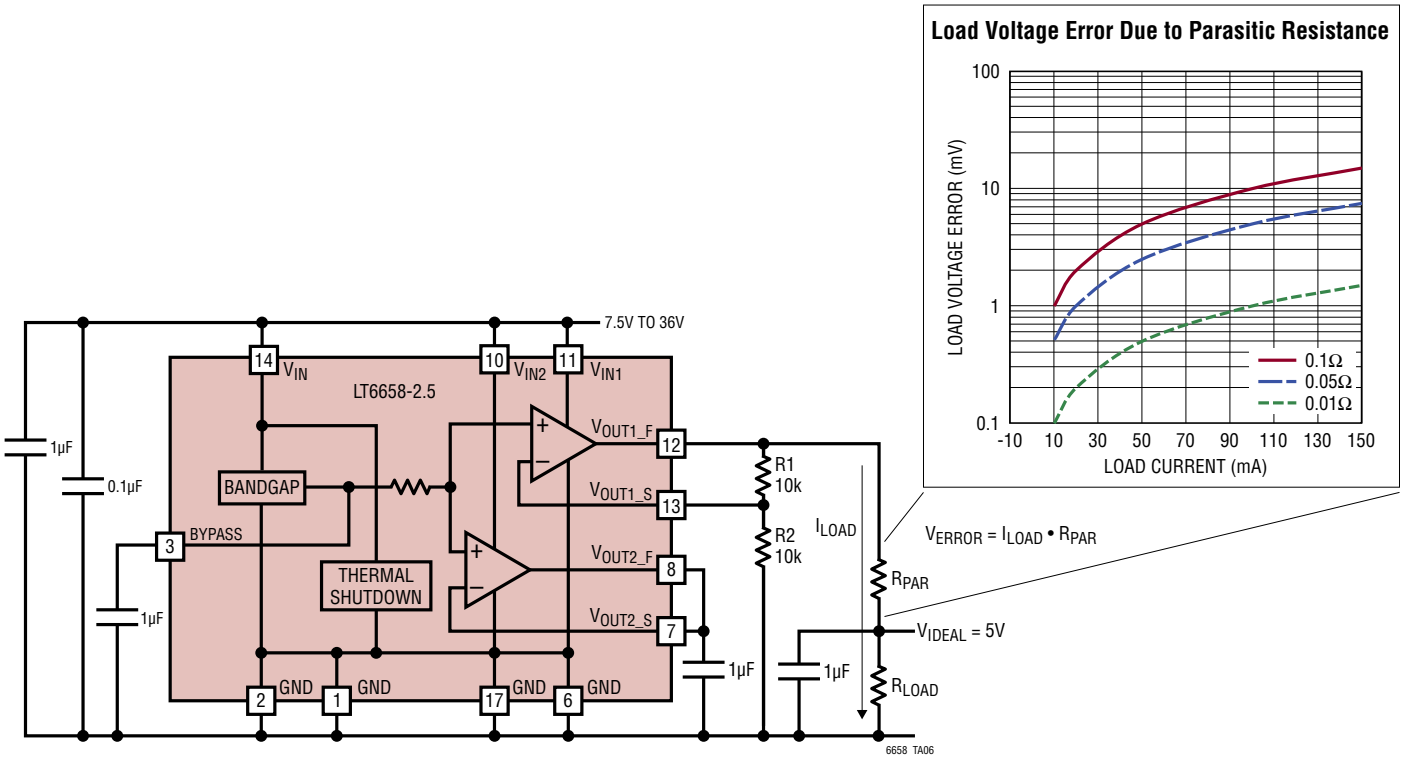
LT6658 Driving Two Code Dependent DAC Reference Inputs. Separate DAC Reference Biasing Eliminates Code Dependent Reference Current Interaction



*R_{PAR} IS THE PARASITIC RESISTANCE OF THE BOARD TRACE AND SHOULD BE > 0.048Ω TO MAINTAIN GOOD INL

TYPICAL APPLICATIONS

Common Errors for Non-Unity Gain Applications



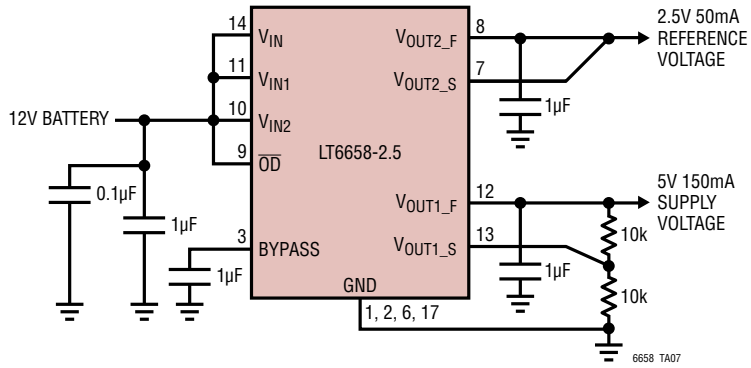
KELVIN SENSE ERROR: R_{PAR} WILL CAUSE AN ERROR $V_{ERROR} = I_{LOAD} \bullet R_{PAR}$.
CONNECT THE TOP OF R1 DIRECTLY TO THE TOP OF R_{LOAD}.
RESISTOR TOLERANCE ERROR: GAIN NETWORK ERROR CAN BE REDUCED BY USING A MATCHED RESISTOR NETWORK SUCH AS THE LT5400.

R1 AND R2 TOLERANCE (%)	R_{PAR} (Ω)	I_{LOAD} (mA)	± ERROR (mV)
1	0.05	0	35.4
1	0.05	150	42.9
0.1	0.05	0	3.5
0.1	0.05	150	11.0
0.1	0.02	150	6.5
0.1	0.01	150	5.0

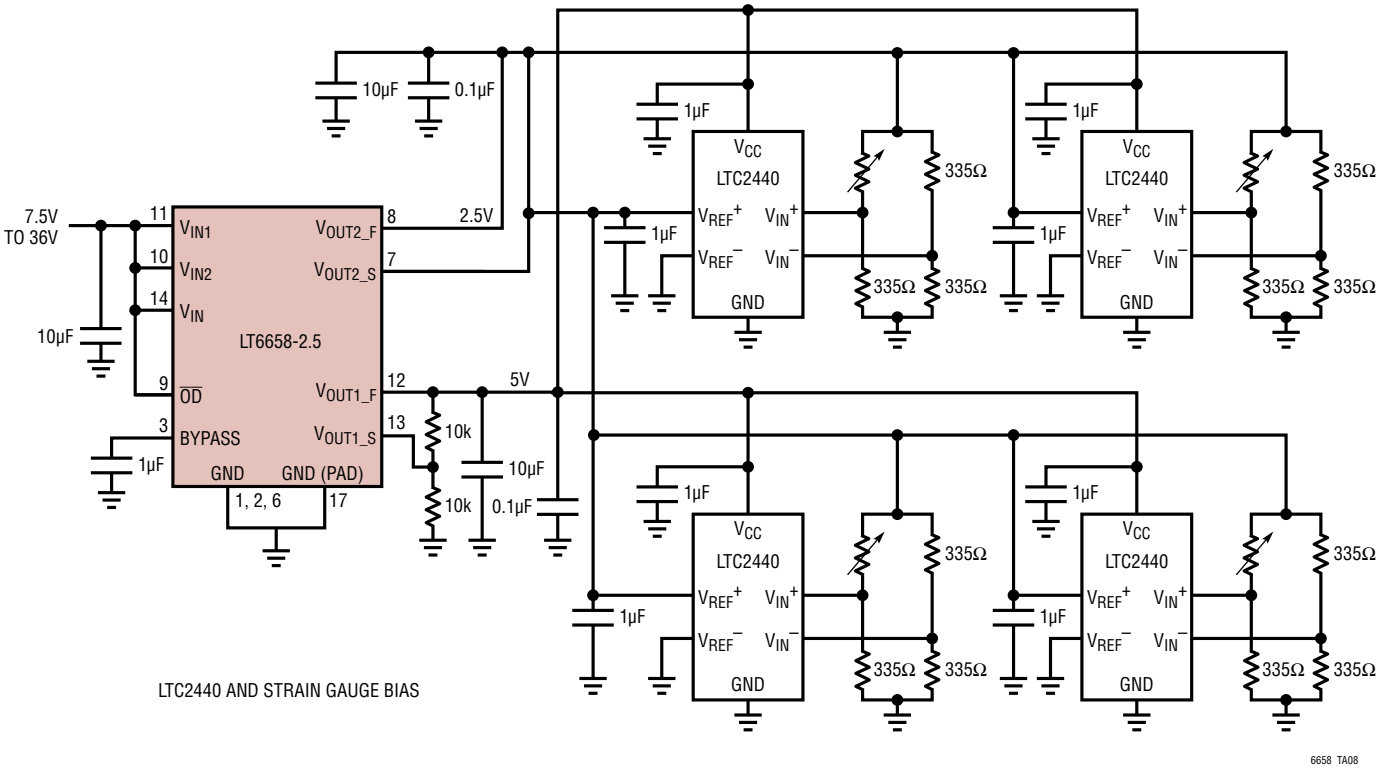
R1 AND R2 TOLERANCE ERRORS ADDED ROOT-SUM-SQUARE

TYPICAL APPLICATIONS

Automotive Reference and Supply Voltage Application

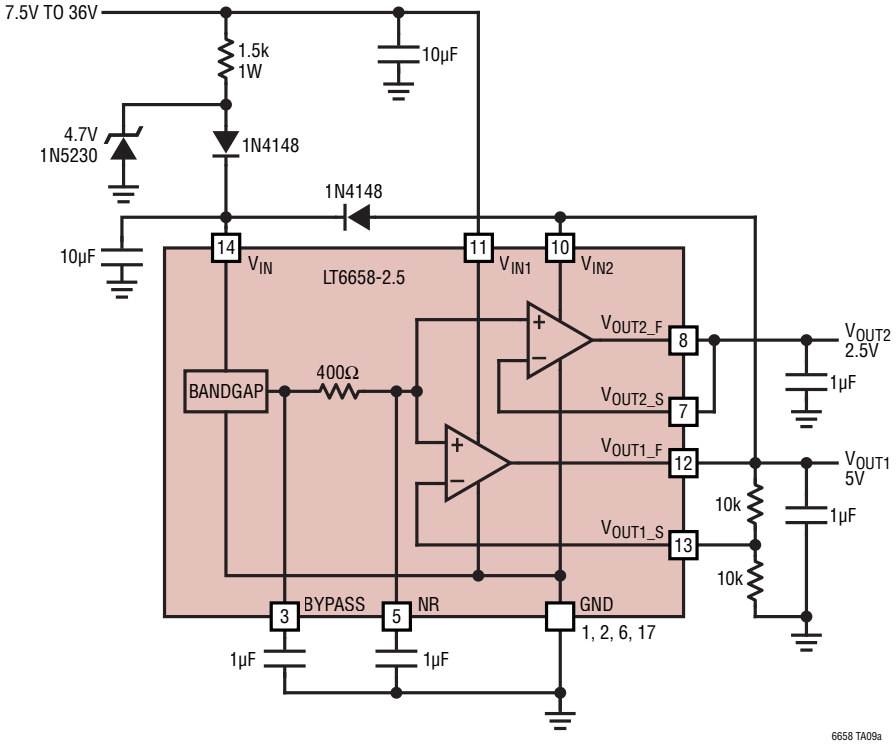


LT6658 Biasing Multiple Strain Gauges

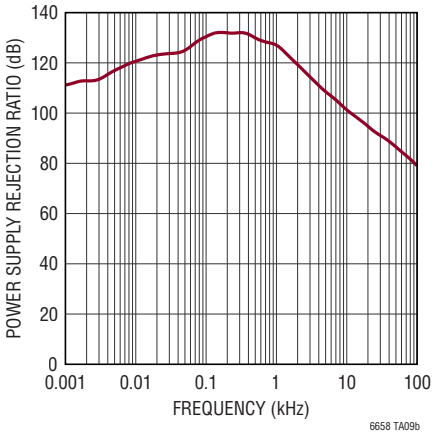


TYPICAL APPLICATIONS

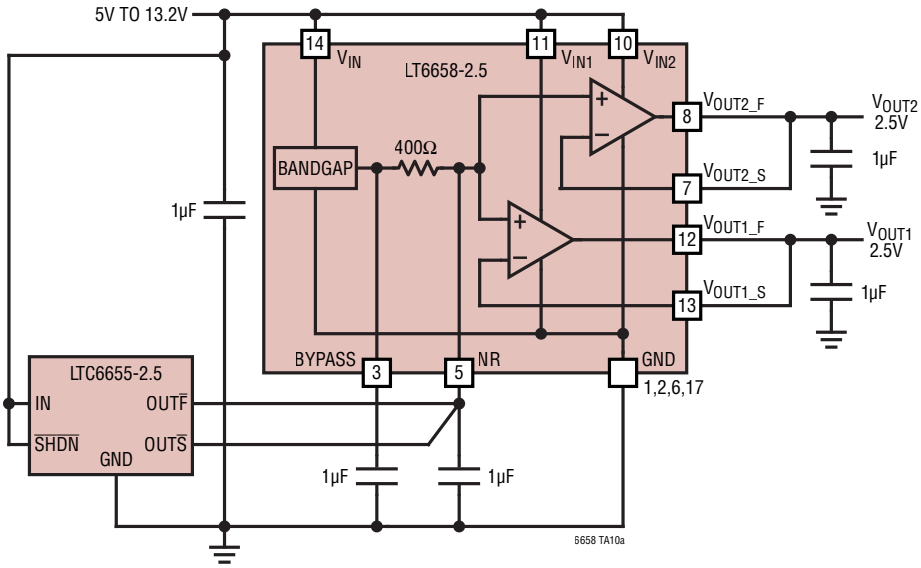
Recursive Reference Application (V_{OUT1} Supplies Power to V_{IN} and V_{IN2})



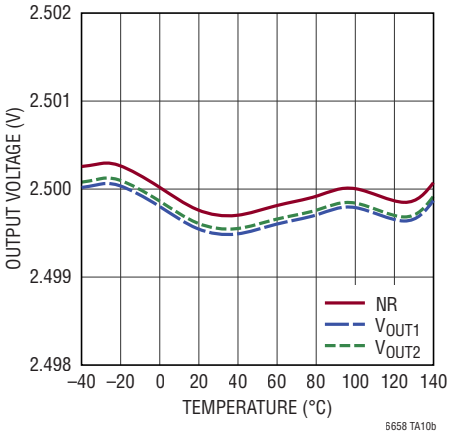
Recursive Reference Power Supply Rejection Ratio



Low Drift Regulator Application



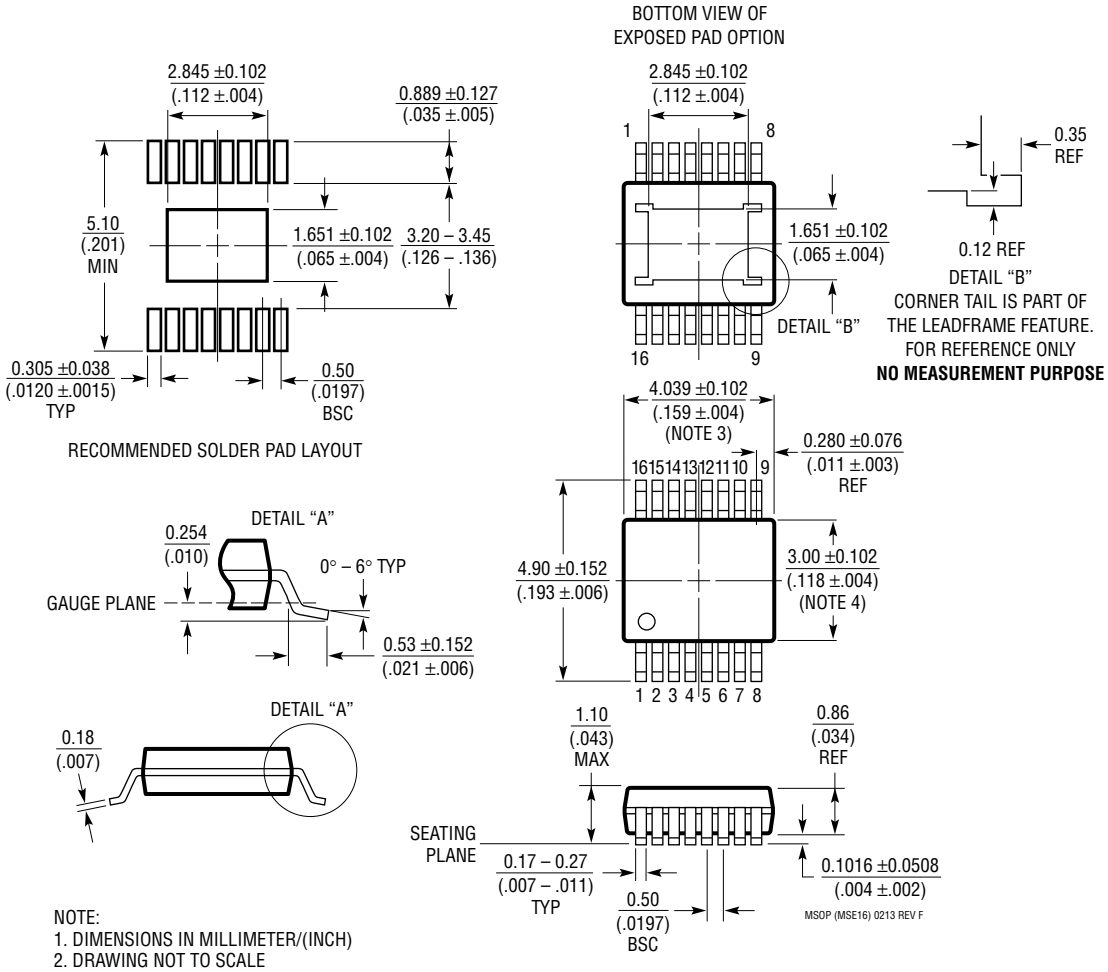
Precision Low Drift Application Drift = 1.5ppm/°C; –40°C to 125°C



PACKAGE DESCRIPTION

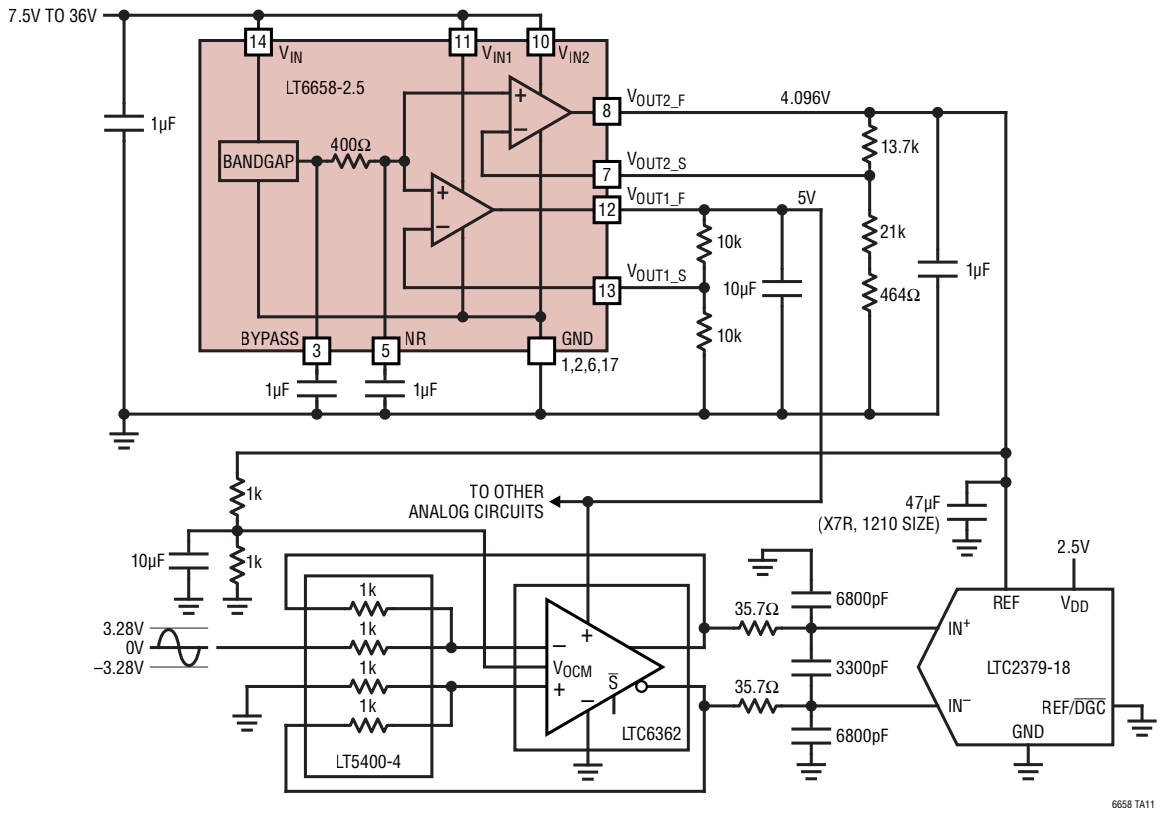
Please refer to http://www.linear.com/product/LT6658#packaging for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1460	Micropower Series References	20mA Output Drive, 0.075% Accuracy, 10ppm/°C Drift
LT1461	Precision Low Dropout Series References	50mA Output Drive, 0.04% Accuracy, 3ppm/°C Drift, 50µA Supply Current, 300mV Dropout
LT6654	All Purpose, Rugged and Precise Series References	±10mA Output Drive, 0.05% Accuracy, 10ppm/°C Drift, 100mV Dropout, 1.6ppm$_{P-P}$ Noise (0.1Hz to 10Hz), –55°C to 125°C
LTC6655	Precision Low Noise Series References	±5mA Output Drive, 0.025% Accuracy, 2ppm/°C Max, 0.25ppm$_{P-P}$ Noise (0.1Hz to 10Hz), –40°C to 125°C
LT6660	Tiny Micropower Series References	20mA Output Drive, 0.2% Accuracy, 20ppm/°C Drift, 2mm × 2mm DFN Package
LT1761	Low Noise Low Dropout Linear Regulator	100mA Output Drive, 300mV Dropout, V_{IN} = 1.8V to 20V, 20µV_{RMS} Noise (10Hz to 100kHz), ThinSOT™ package
LT3042	Ultralow Noise, Ultrahigh PSRR Linear Regulator	200mA Output Drive, 350mV Dropout, V_{IN} = 1.8V to 20V 0.8µV_{RMS} Noise (10Hz to 100kHz), 79dB PSRR (1MHz)
LT3050	Low Noise Linear Regulator with Current Limit and Diagnostic Functions	100mA Output Drive, 300mV Dropout, V_{IN} = 2V to 45V, 30µV_{RMS} Noise (10Hz to 100kHz), 50µA Supply Current, Adj. Output
LT3060	Micropower, Low Noise, Low Dropout Linear Regulator	100mA Output Drive, 300mV Dropout, V_{IN} =1.7V to 45V, 30µV_{RMS} Noise (10Hz to 100kHz), 40µA Supply Current, Adj. Output
LT3063	Micropower, Low Noise, Low Dropout Linear Regulator with Output Discharge	200mA Output Drive, 300mV Dropout, V_{IN} =1.6V to 45V, 30µV_{RMS} Noise (10Hz to 100kHz), 40µA Supply Current

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